

1

2

3

4

Compal Confidential

B3ZMS MB Schematic Document

LA-D591P

Rev: 2.0

2016.02.24

DAX1

Part Number	Description
DAA000C2000 B3ZMS_PCB_REV01	PCB 1JL LA-D591P REV0 MB 1

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				Date: Wednesday, February 24, 2016	B3ZMS LA-D591P	2.0
				Sheet 1 of 45		

HDMI Conn.



HDMI
PS8407A

page 22

DDI2
HDMI x 4 lanes

eDP



page 21

eDP

DDI



NGFF
WLAN
USB port 5



PCIe 1.0
2.5GT/s
port 6

PCIe 1.0
2.5GT/s
port 5

Card Reader
RTS5220

page 26

Card Reader
2 in 1 (SD)



page 26

RTC CKT.

page 14

Power On/Off CKT.

page 39

DC/DC Interface CKT.

page 42

Power Circuit DC/DC

page 43~55

Sub Board

LS-D592P
IO/B

page 26

Intel Skylake U

Skylake U
Skylake PCH-LP(MCP)
(SKL-U_2+2)

Processor

Dual Core + GT2

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NGFF2280
SSD

page 23

Flexible IO

SATA3.0
6.0 Gb/s
port 7
(SATA0)

15W
1356pin BGA

page 06~17

LPC/eSPI BUS

CLK=24MHz

ENE
KB9022/9032

page 27

iTPM

Int.KBD



page 28

Touch Pad
PS2 (from EC) / I2C (from SOC)



page 28

Memory Bus
1.2V lpmddr3 1600MHz

CH_A

LPDDR3 Memory down P.18

CH_B

LPDDR3 Memory down P.19

USB 3.0
Type-C x1
USB port 3,4



page 25

USB 3.0
conn x2
USB port 1,2



page 24

BlueTooth
USB port 5



page 26

CMOS
Camera
USB port 7



page 21

USBx8 48MHz

HD Audio

3.3V 24MHz

SPI

SPI ROM x2

page 8

HDA Codec
ALC255

page 26

Int. Speaker

page 26

Int. MIC

page 26

UAI
on Sub/B

page 26



Fan Control

page 29

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				Custom	B3ZMS LA-D591P	2.0
				Date:	Wednesday, February 24, 2016	Sheet 2 of 45

Board ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	V _{BI} D min	V _{BI} D typ	V _{BI} D max	EC AD3
0	0	0 V	0 V	0.300 V	0x00 - 0x0B
1	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x0C - 0x1C
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1D - 0x26
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x27 - 0x30
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3B
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3C - 0x46
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x47 - 0x54
7	56K +/- 1%	1.149 V	1.185 V	1.200 V	0x55 - 0x64

BOM Structure Table

BOM Option Table		BOM Option Table	
Item	BOM Structure	Item	BOM Structure
Unpop	@	CODEC(ALC255)	255@
Connector	CONN@	CODEC(ALC83)	283@
EMC requirement	EMC@		
EMC requirement depop	@EMC@		
LPC MODE for EC	LPC@		
ESPI MODE for EC	ESPI@		
For Acer IOAC	IOAC@		
No Acer IOAC	NIOAC@		
For Skylake-U	SKL@		
For KabyLake-U	KBL@		
SPI ROM 8M*1	8M_SINGLE@		
TPM	TPM@	DRAM BOM Select	X76@/X7601@ ~ X7614@
DMIC*1	1DMIC@		
For ES Sampel Only	ES@	CPU Code	Q5:QJ8Q@,QJKK@, QJKA@,QJKA@,MP:SR2EU@,SR2EY@
Keyboard backlight	KB@		
Finger Print	FP@		

I2C Address Table

BUS	Device	Address(7 bit)	Address(8bit)	
			Write	Read
I2C_0 (+3VS)	Reserved (Touch Panel)			
I2C_1 (+3VS)	TM-P2969-001 (TP)	0x2C		
	SB8787-1200 (TP-ELAN)	0x15		
	DIMM1	0xA0		
SOC_SMBCLK +3VS	DIMM2	0xA4		
	LIS3DHTR(G-Sensor)	0x30		
SOC_SML1CLK +3VS	N16S-GT (VGA)	0x9E		
	PCH-LP (SOC)	0x90		
	BQ24780 (Charger IC)	0x12		
EC_SMB_CK1 +3VLP	BATTERY PACK	0x16		

43 level BOM table

43 Level	Description	BOM Structure
431A1MBOL06	PCBA MB AD591 B3ZMS I36100U SR2EU 4G HDMI	8M_SINGLE@/EMC@/SKL@/KB@/LPC@/IOAC@/SR2EU@
431A1MBOL07	PCBA MB AD591 B3ZMS I56200U SR2EY 4GHDMI	8M_SINGLE@/EMC@/SKL@/KB@/LPC@/IOAC@/SR2EY@
431A1MBOL08	PCBA MB AD591 B3ZMS I56200U SR2EY 8GHDMI	8M_SINGLE@/EMC@/SKL@/KB@/LPC@/IOAC@/SR2EY@
431A1MBOL09	PCBA MB AD591 B3ZMS I76500U SR2EZ 4GHDMI	8M_SINGLE@/EMC@/SKL@/KB@/LPC@/IOAC@/SR2EZ@
431A1MBOL10	PCBA MB AD591 B3ZMS I76500U SR2EZ 8GHDMI	8M_SINGLE@/EMC@/SKL@/KB@/LPC@/IOAC@/SR2EZ@
431A1MBOL11	SMT MB AD591 B3ZMS PMD4405USR2EX 4G	8M_SINGLE@/EMC@/SKL@/KB@/LPC@/IOAC@/SR2EX@

Power State

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	0.1(Skylake)
1	0.2(Skylake)
2	1.0(Skylake)
3	2.0(Skylake)
4	
5	
6	
7	2.0(KabyLake)

Voltage Rails

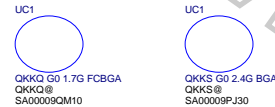
Power Plane	Description	S0	S3	S4/S5
+19V_VIN	Adapter power supply	N/A	N/A	N/A
+17.4V_BATT	Battery power supply	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VCC_CORE	Processor IA Cores Power Rail	ON	OFF	OFF
+VCC_GT	Processor Graphics Power Rails	ON	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF
+0.6VS_VTT	DDR +0.675VS power rail for DDR terminator .	ON	OFF	OFF
+1.0VALW_PRIM	+1.0V Always power rail	ON	ON	ON*1
+1.0V_VCCSTU	Sustain voltage for processor in Standby modes	ON	ON	OFF
+VCCIO	CPU IO power rail	ON	OFF	OFF
+1.0VS_VCCSTG	+1.0VALW_PRIM Gated version of VCCST	ON	OFF	OFF
+1.5V_VDD2	DDR3/4 +1.35V Power Rail	ON	ON	OFF
+1.8V_ALW_FRM	+1.8V Always power rail	ON	ON	ON*1
+1.5V3	System +1.8V power rail	ON	OFF	OFF
+3VLP	+1.5V to +3VLP power rail for suspend power	ON	ON	ON
+3VALW	+3V to +3VALW always on power rail	ON	ON	ON*1
+3VS	+3V to +3VS power rail	ON	OFF	OFF
+5VALW	+5V Always power rail	ON	ON	ON
+5VS	System +5V power rail	ON	OFF	OFF
+RTCVCC	RTC Battery Power	ON	ON	ON

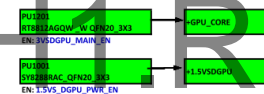
Note : ON*1 means power plane is ON only when WOL enable and RTC wake at BIOS setting, otherwise it is OFF.

Skylake CPU

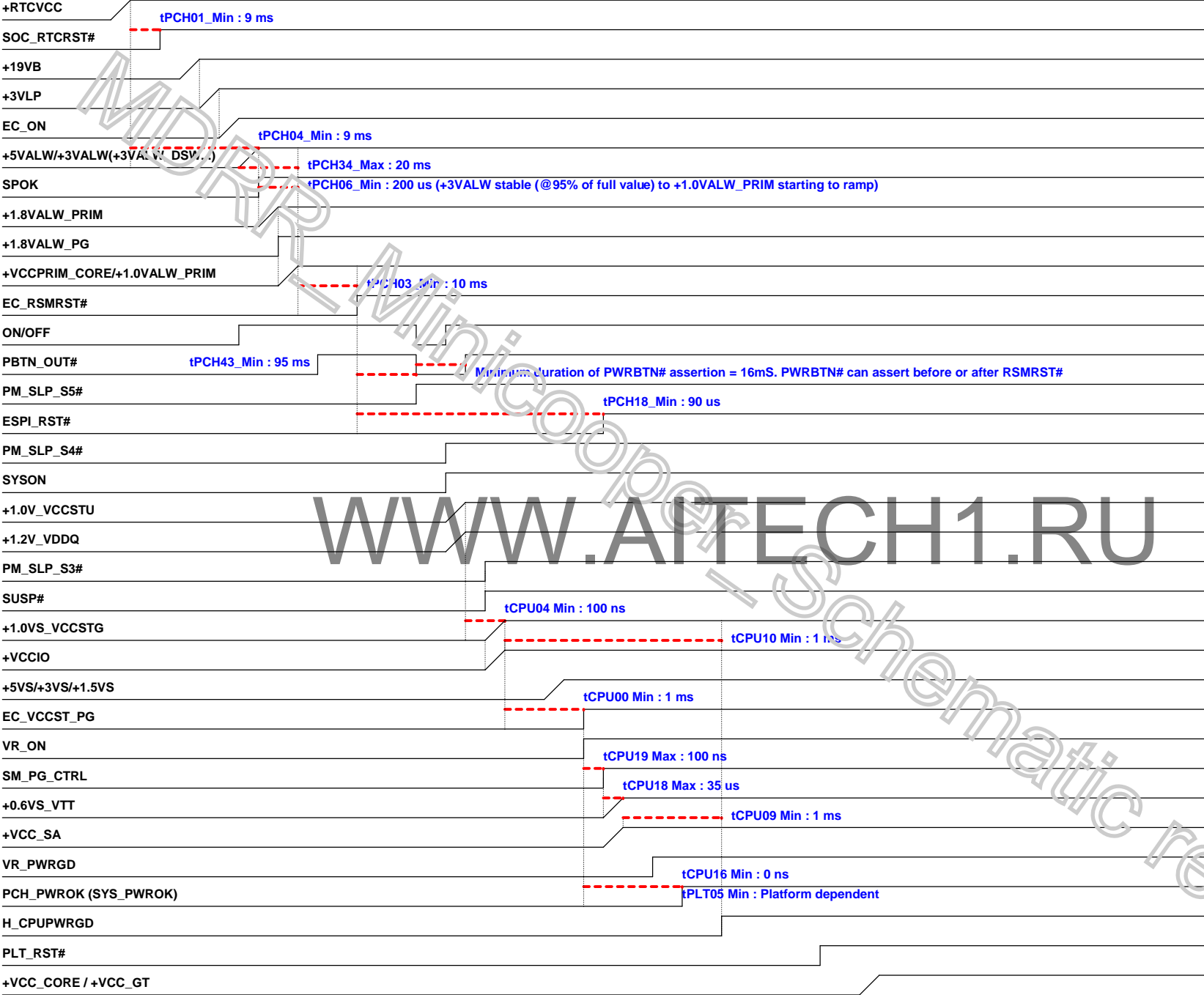


KabyLake CPU





PWR Sequence_SKL-U2+2_DDR3L_Value_NON CS



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					Power Sequence
					Document Number
					B3ZMS LA-D591P
					Rev
					2.0
					Date: Wednesday, February 24, 2016
					Sheet 5 of 45

SOC_DP1_CTRL_DATA(Internal Pull Down):

Display Port B Detected

0 = Port B is not detected

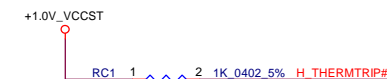
1 = Port B is detected.

SOC_DP2_CTRL_DATA(Internal Pull Down):

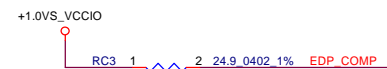
Display Port C Detected

0 = Port C is not detected.

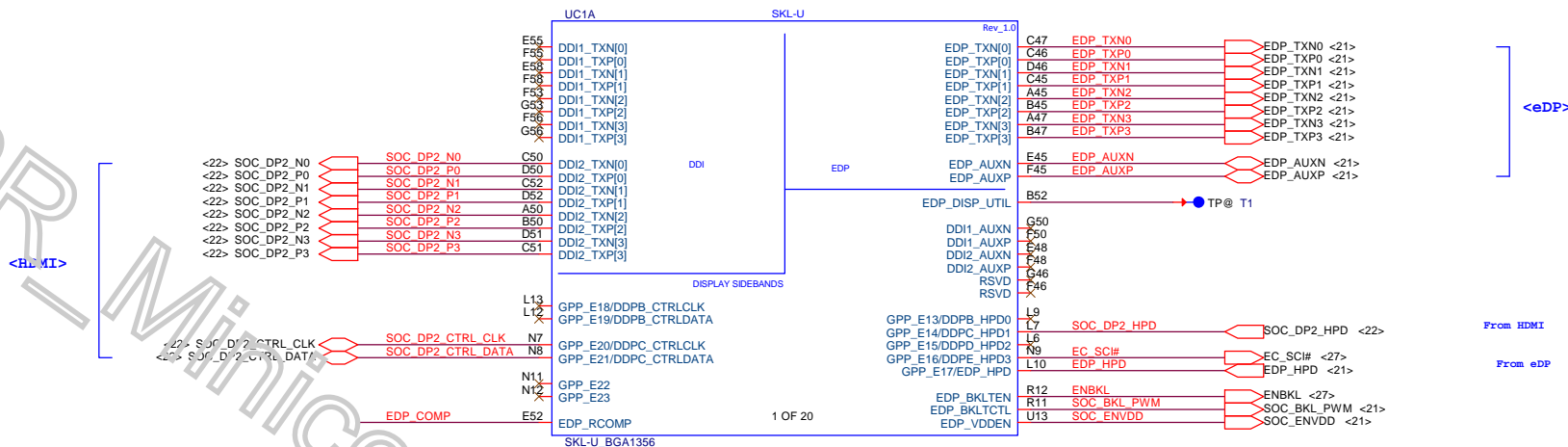
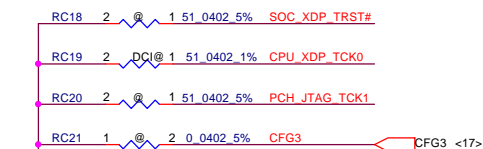
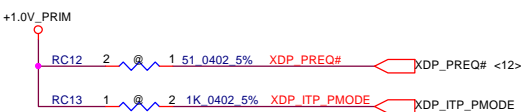
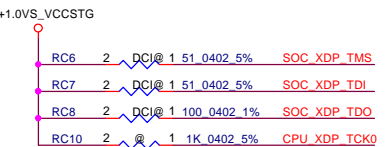
1 = Port C is detected.



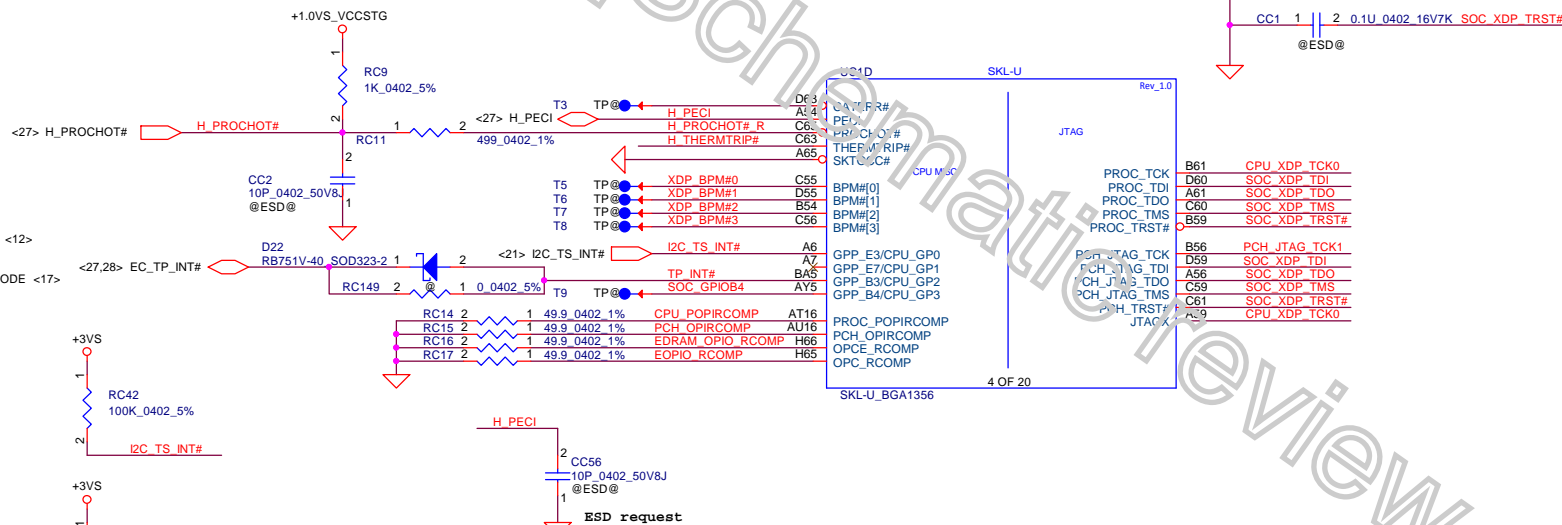
COMPENSATION PU FOR eDP



CAD note:
Trace width=20 mils, Spacing=25mil, Max length=100mils

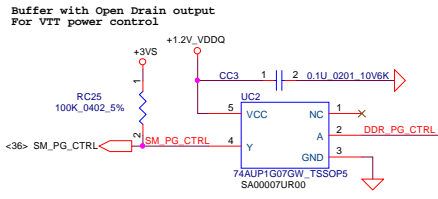


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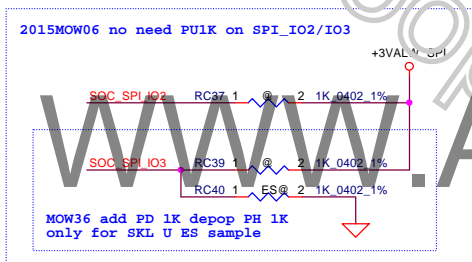
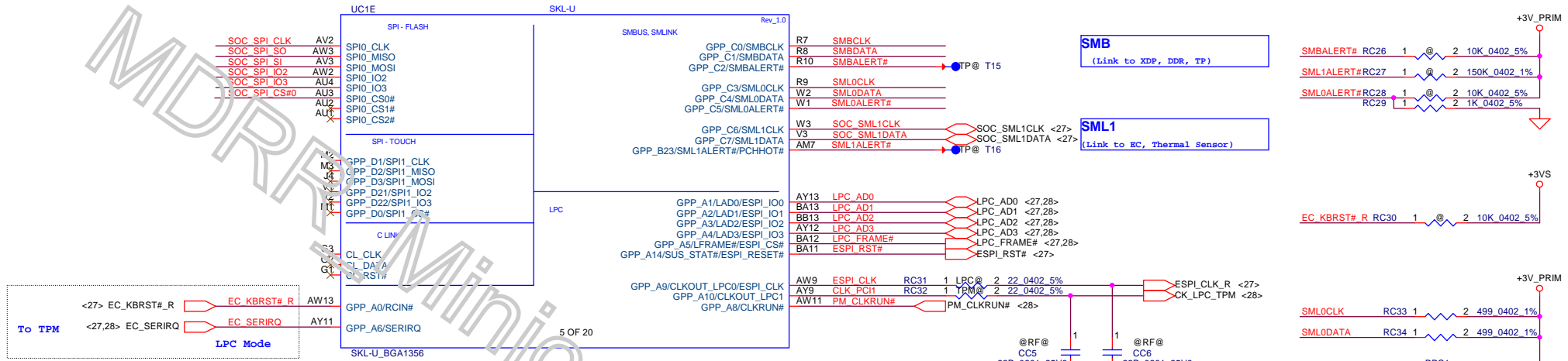
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				B3ZMS LA-D591P				Document Number			
				B3ZMS LA-D591P				Date			
				Wednesday, February 24, 2016				Sheet			
				6				of			
				45				Rev			
				2.0							

non-Interleaved

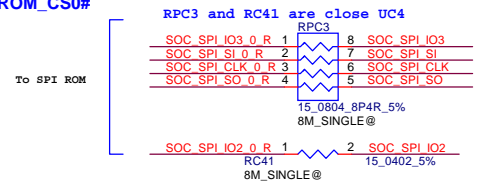


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				Cust	B3ZMS LA-D591P	2.0
				Date:	Wednesday, February 24, 2016	Sheet 7 of 45

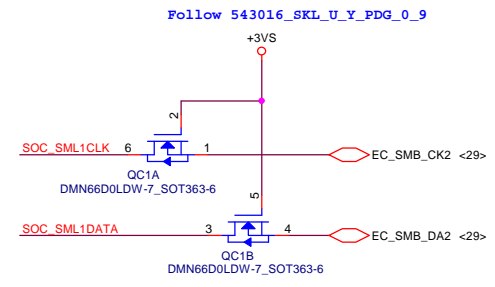
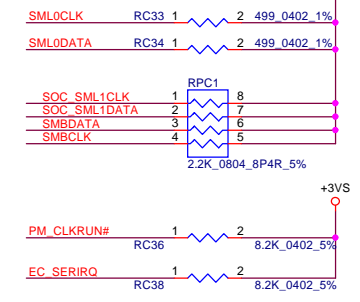
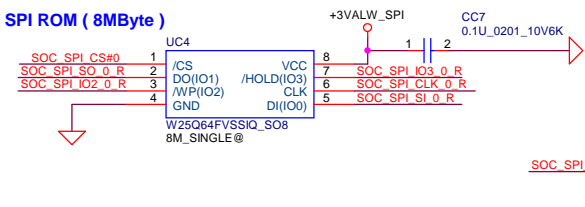
SML0ALERT# (Internal Pull Down):
eSPI or LPC
0 = LPC is selected for EC --> For KB9022/9032 Use
1 = eSPI is selected for EC --> For KB9032 Only.



Single SPI ROM_CS#0



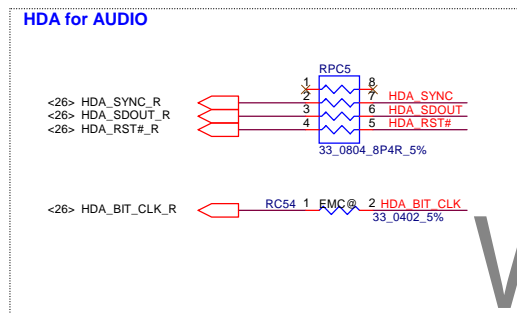
SPI ROM (8MByte)



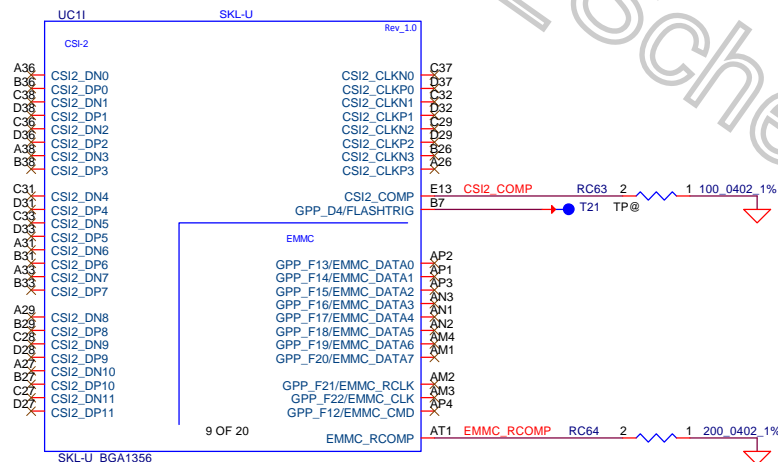
SPI ROM Setting	Bom Option
8M + 2M (Standard Demand)	Single SPI = 2M_SINGLE@(UC2) Dual SPI = 8M_DUAL@
8M + 4M(If Support ISH)	Single = 4M_SINGLE@(UC2) Dual SPI = 8M_DUAL@
8M + 8M(If Support ISH+VPRO)	Single = 8M_SINGLE@(UC2) Dual SPI = 8M_DUAL@
16M	Single = 16M_SINGLE@(UC2)

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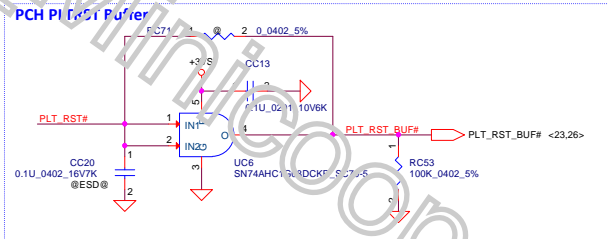
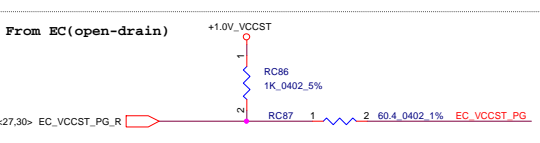
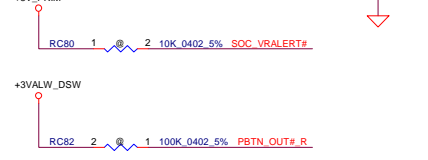
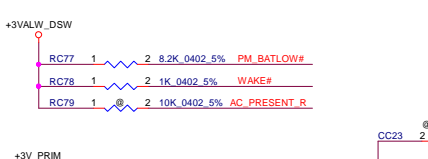
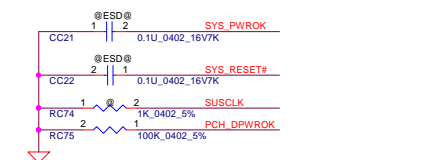
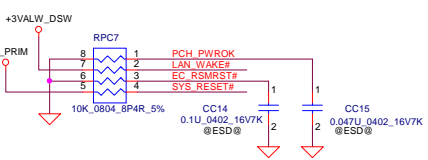
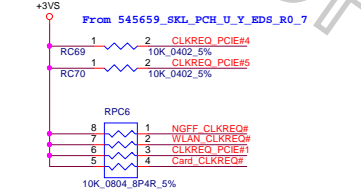
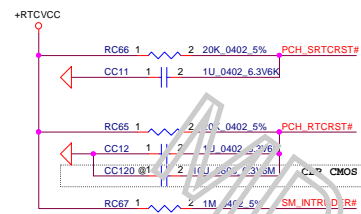
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				Date: Wednesday, February 24, 2016	Rev 2.0
				Sheet 8	of 45



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								Size Custom	Document Number			B3ZMS LA-D591P			Rev 2.0
								Date: Wednesday, February 24, 2016				Sheet 9 of 45			



Only For Power Sequence Debug

T23 TP@RC76

EC_VCCST_PG

EC_VCCST_PG

EC_VCCST_PG

EC_VCCST_PG

EC_VCCST_PG

EC_VCCST_PG

EC_VCCST_PG

EC_VCCST_PG

EC_VCCST_PG

EC_VCCST_PG

EC_VCCST_PG

EC_VCCST_PG

EC_VCCST_PG

EC_VCCST_PG

EC_VCCST_PG

EC_VCCST_PG

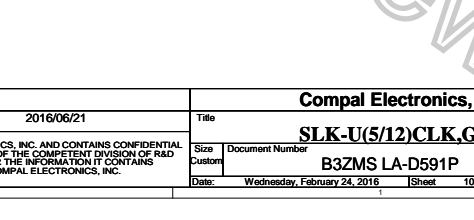
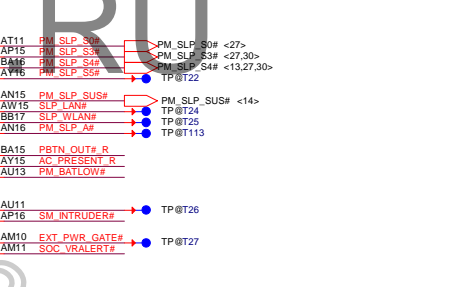
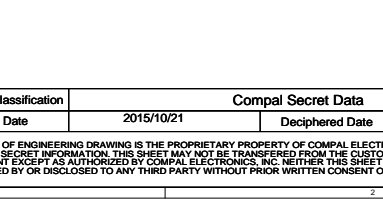
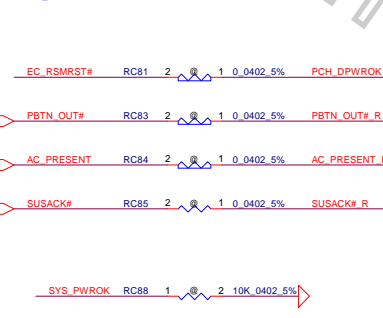
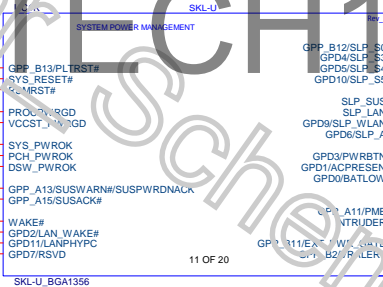
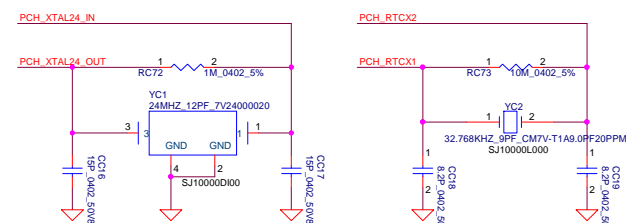
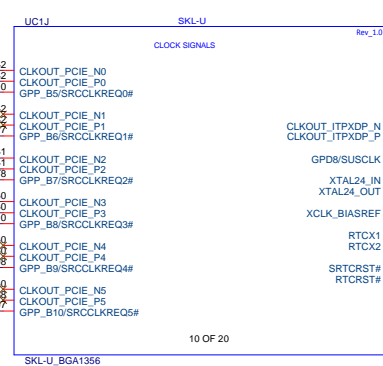
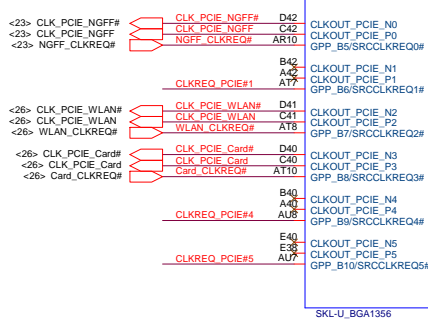
EC_VCCST_PG

EC_VCCST_PG

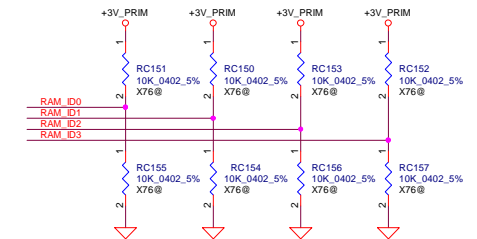
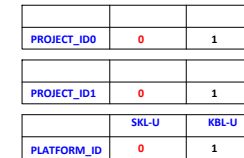
EC_VCCST_PG

EC_VCCST_PG

EC_VCCST_PG

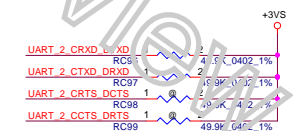
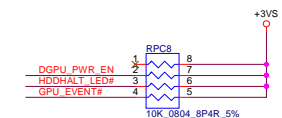


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/10/21	Deciphered Date	2016/06/21	Title	SLK-U(5/12)CLK,GPIO
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				Custom	B3ZMS LA-D591P
				Date	Wednesday, February 24, 2016
				Sheet	10 of 45



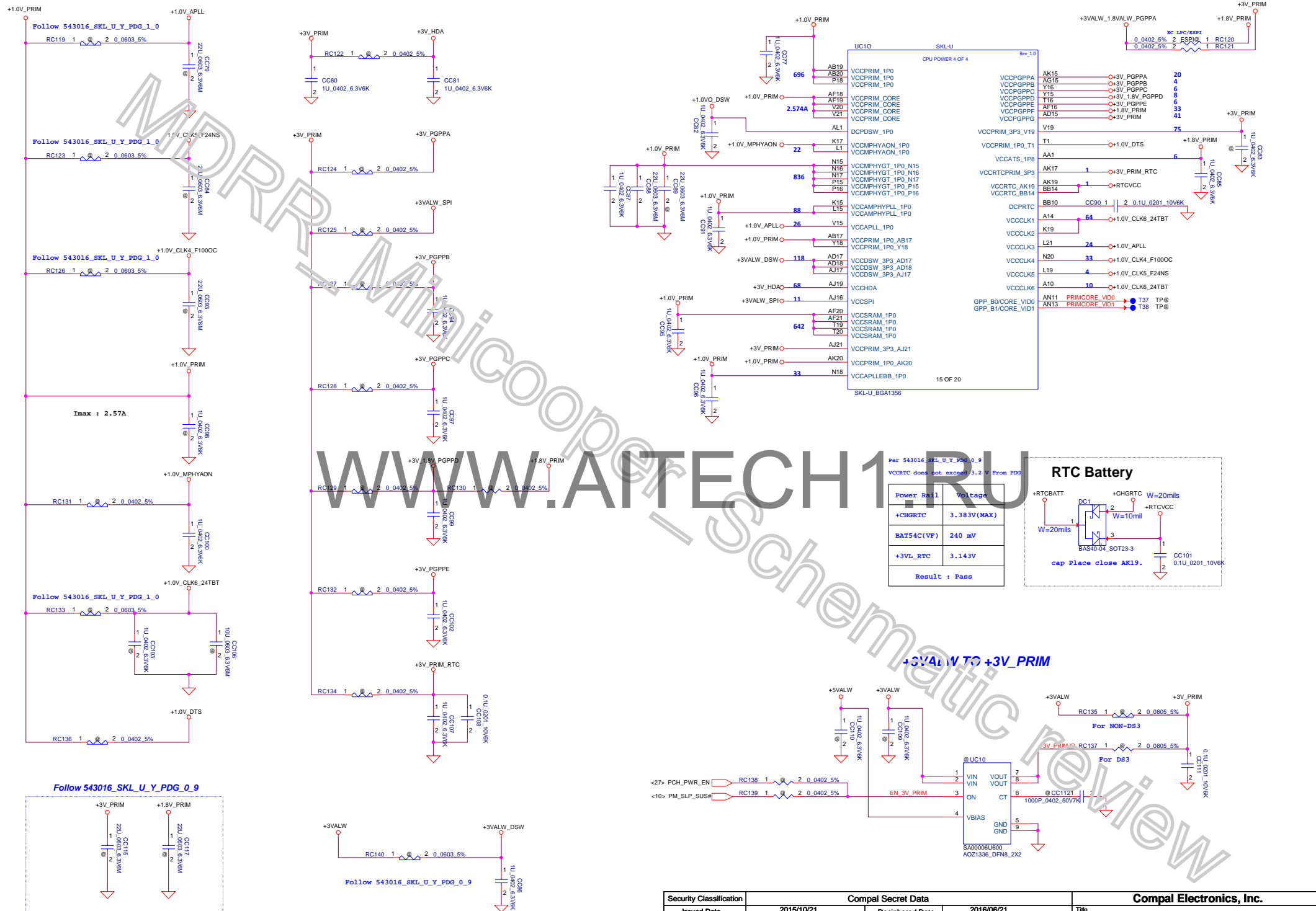
X76669BOL01
X76669BOL03
X76669BOL02
X76669BOL04

1 = LPC Mode

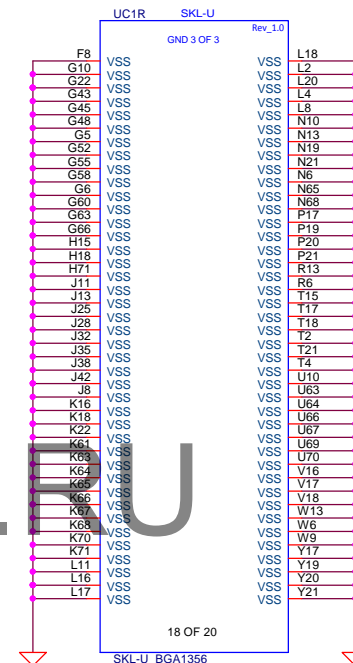



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Issued Date	2015/10/21	Deciphered Date	2016/06/21	Title SKL-U(6/12)GPIO			
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				Custom	B3ZMS LA-D591P	2.0	
				Date:	Wednesday, February 24, 2016	Sheet 11 of 45	

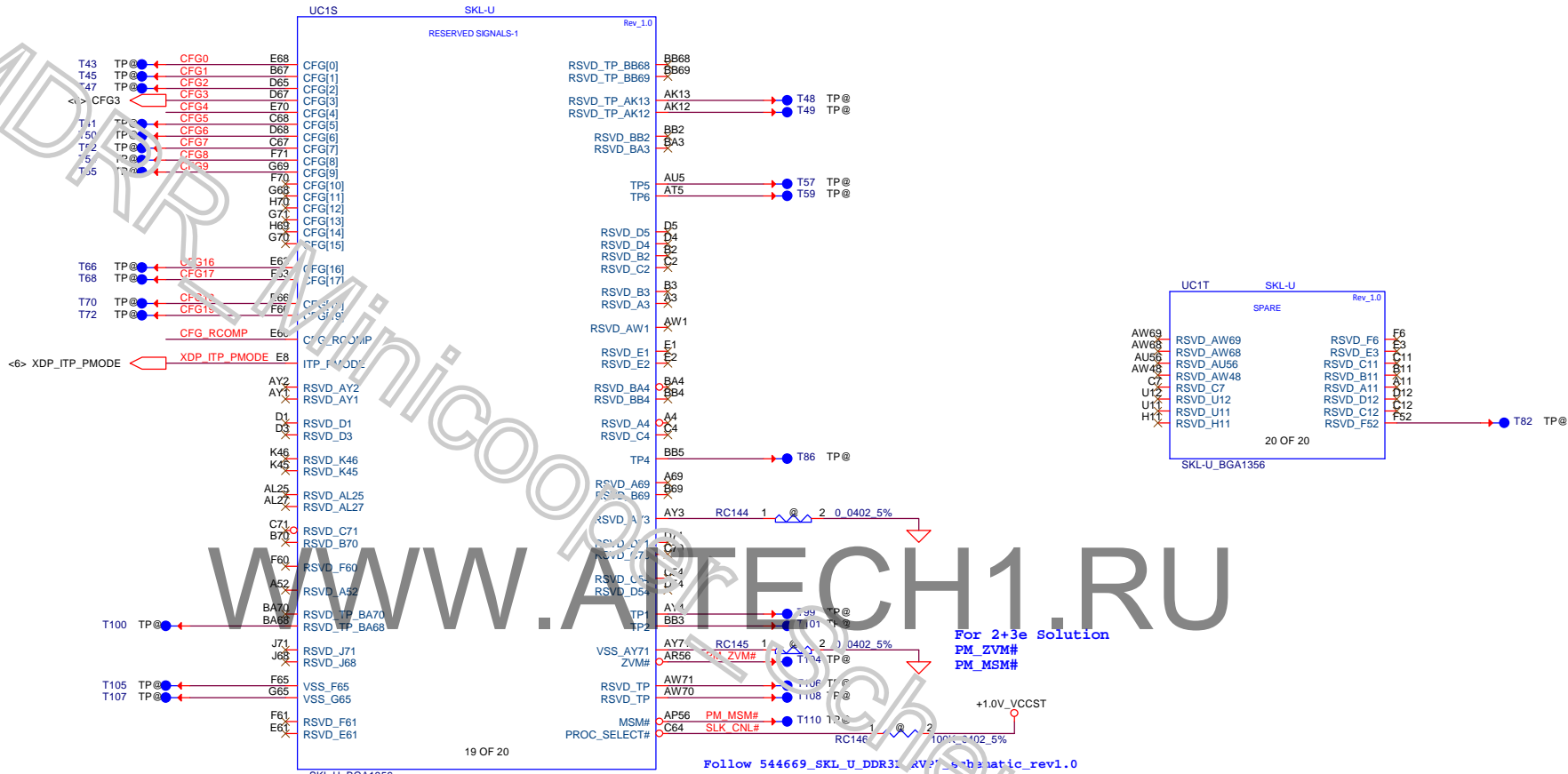
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2015/10/21	Deciphered Date	2016/06/21	Title	SKL-U(8/12)POWER	
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				Date:	Wednesday, February 24, 2016	Sheet 13 of 45



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Issued Date	2015/10/21	Deciphered Date	2016/06/21	Title	SKL-U(9/12)Power
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				Custom	B3ZMS LA-D591P
				Date	Wednesday, February 24, 2016
				Sheet	14 of 45
				Rev	2.0

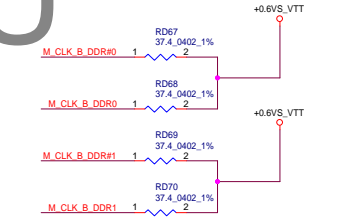
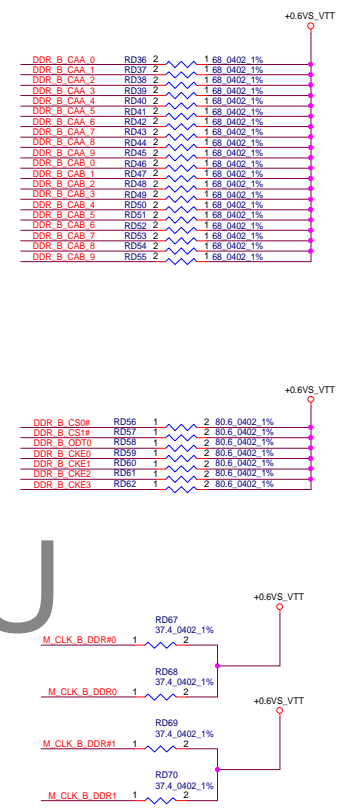
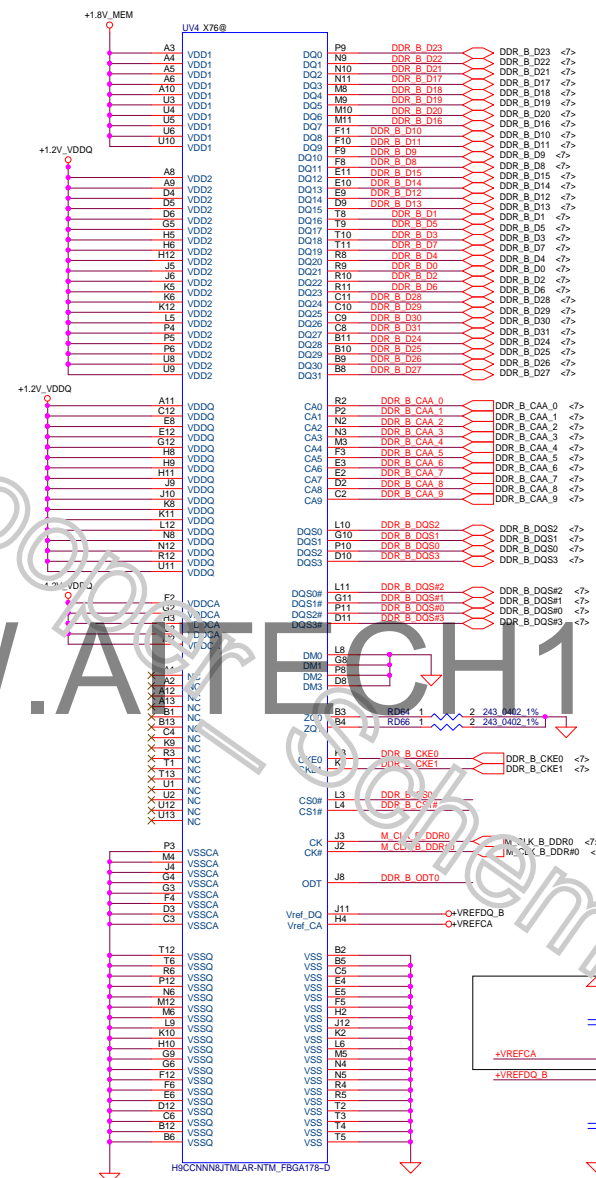
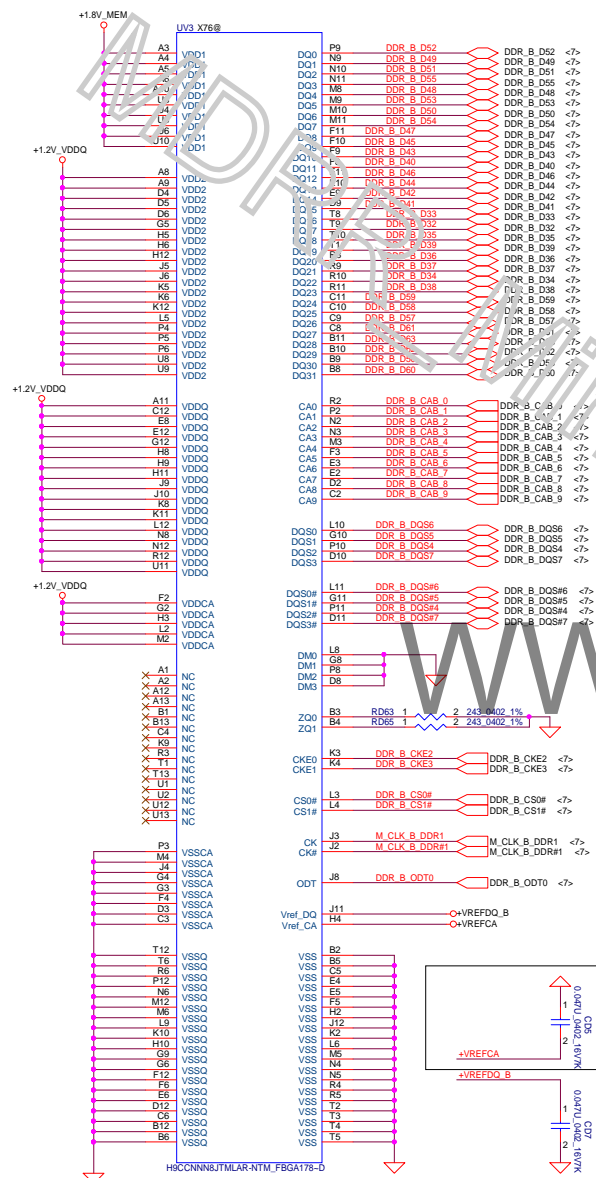


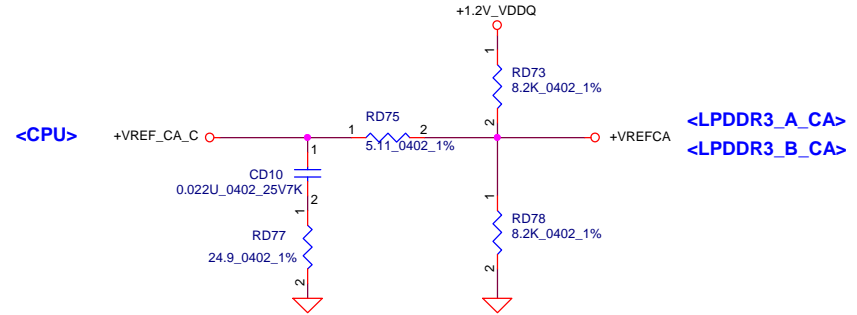
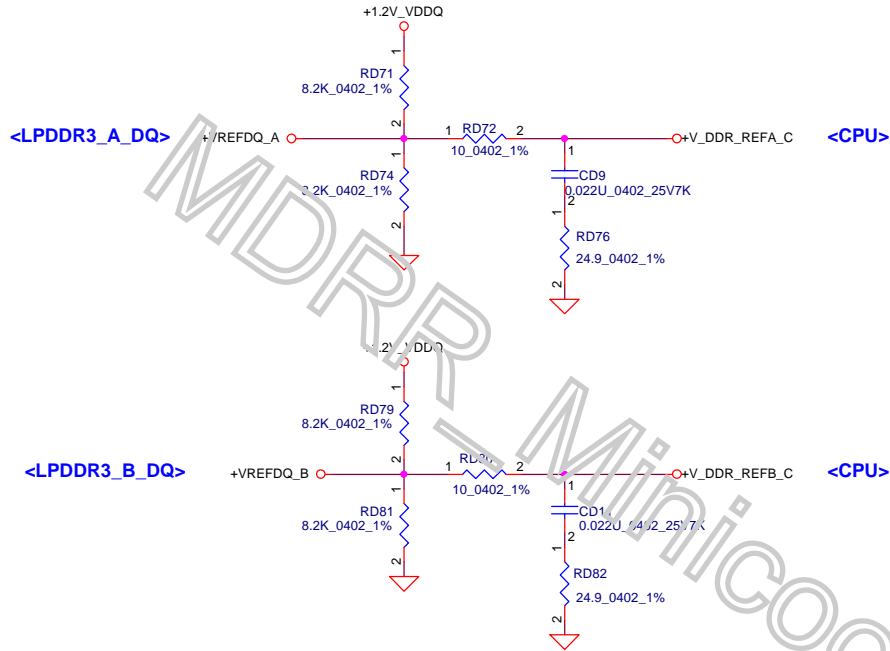
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Issued Date	2015/10/21	Deciphered Date	2016/06/21	Title		
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				Size	Document Number	Rev
				B3ZMS LA-D591P		
Date: Wednesday, February 24, 2016				Sheet	16 of 45	



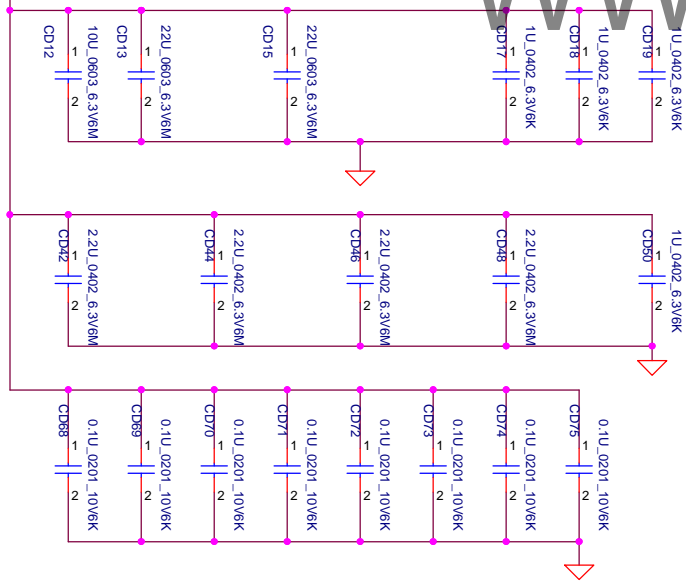
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

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Size	Document Number	B3ZMS LA-D591P		Rev	2.0
Date	Wednesday, February 24, 2016	Sheet	17	of	45

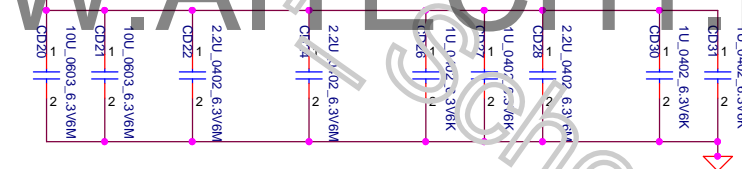




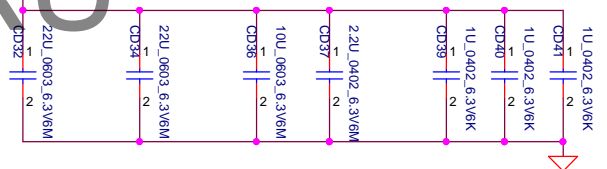
VDDQ DECAPS (10UF * 5 / 1UF * 12 / 0.1UF * 8)



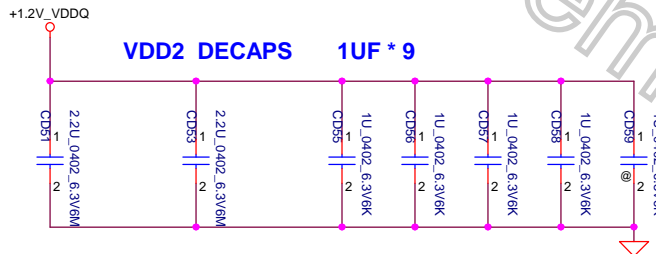
VTT DECAPS (1UF * 2 / 1UF * 10)



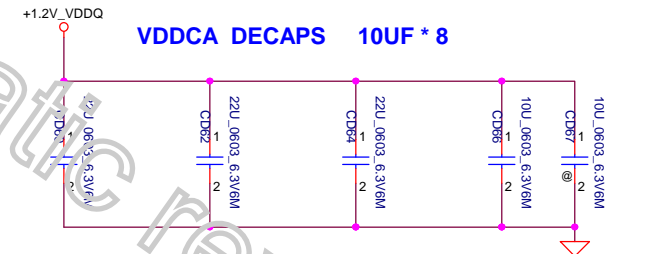
VDD1 DECAPS (10UF * 5 / 1UF * 5)



VDD2 DECAPS 1UF * 9

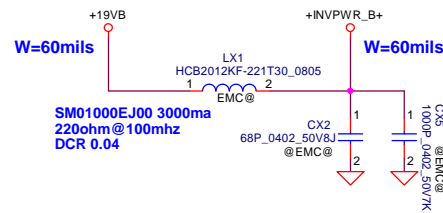
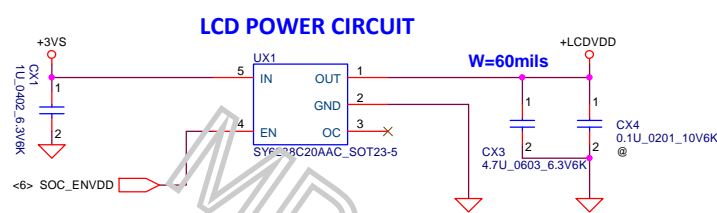


VDDCA DECAPS 10UF * 8

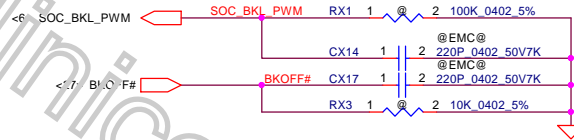
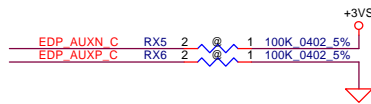
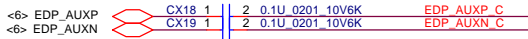
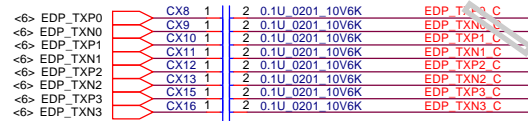


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				B32MS LA-D591P	
				Date:	Wednesday, February 24, 2016
				Page	20 of 45

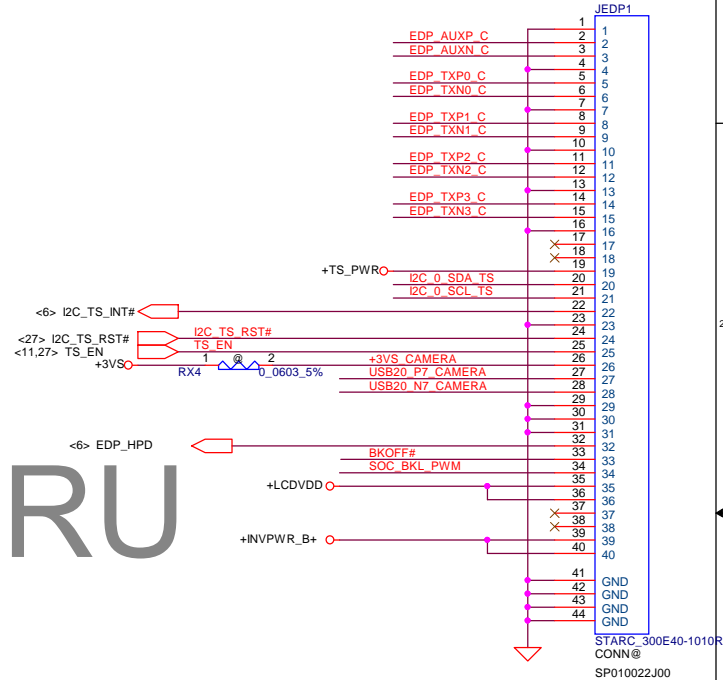
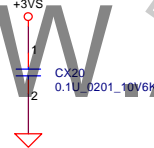
LCD POWER CIRCUIT



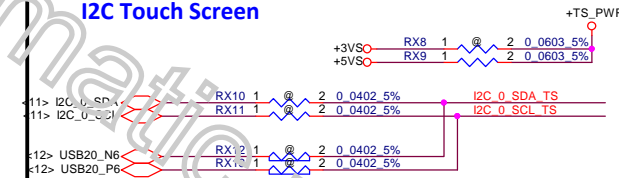
LCD/LED PANEL Conn.



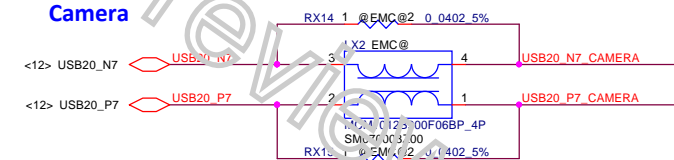
Place closed to EDP1



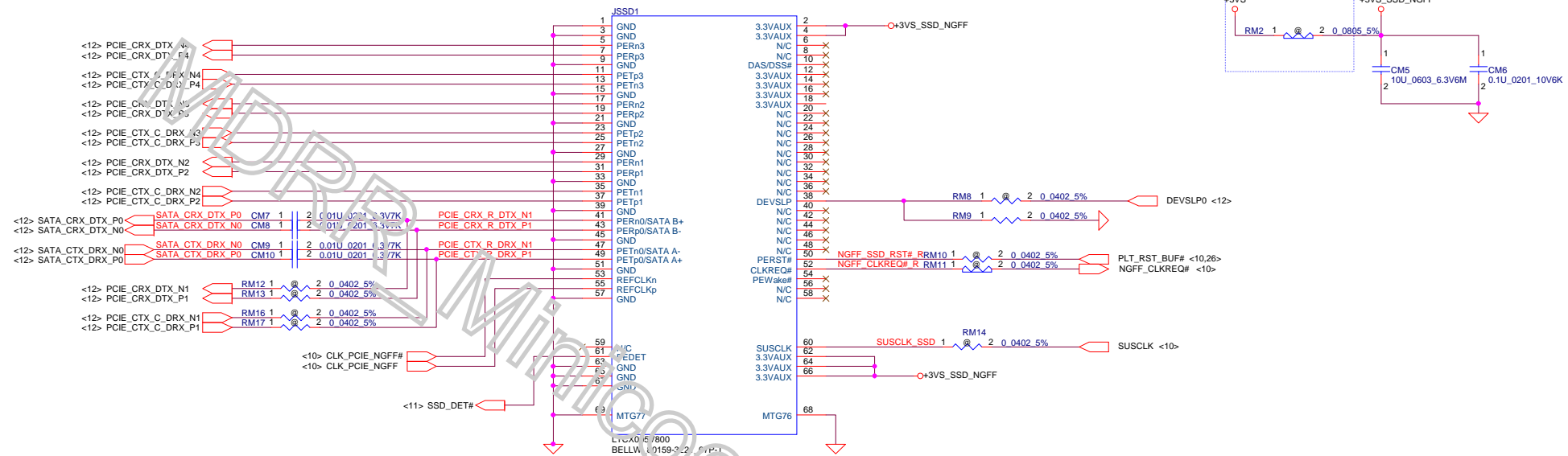
I2C Touch Screen



Camera



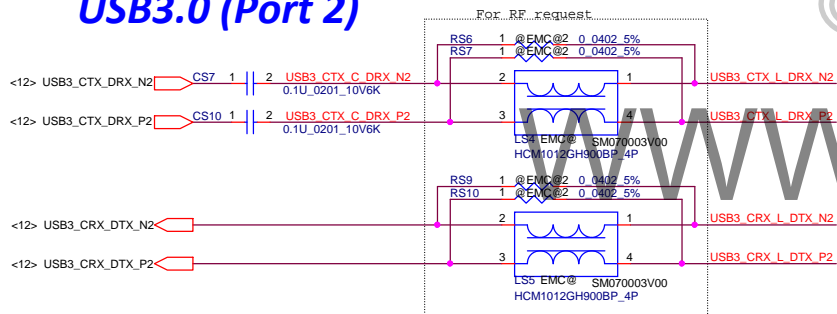
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
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2015/10/21				2016/06/21				eDP Connector			
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B3ZMS LA-D591P				2.0				Date			
Wednesday, February 24, 2016				Sheet				21 of 45			



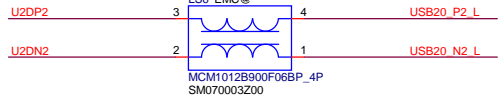
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										mSATA & NFC	
										Document Number	
										B3ZMS LA-D591P	
										Rev	
										2.0	
										Date: Wednesday, February 24, 2016	
										Sheet 23 of 45	

USB3.0 (Port 2)

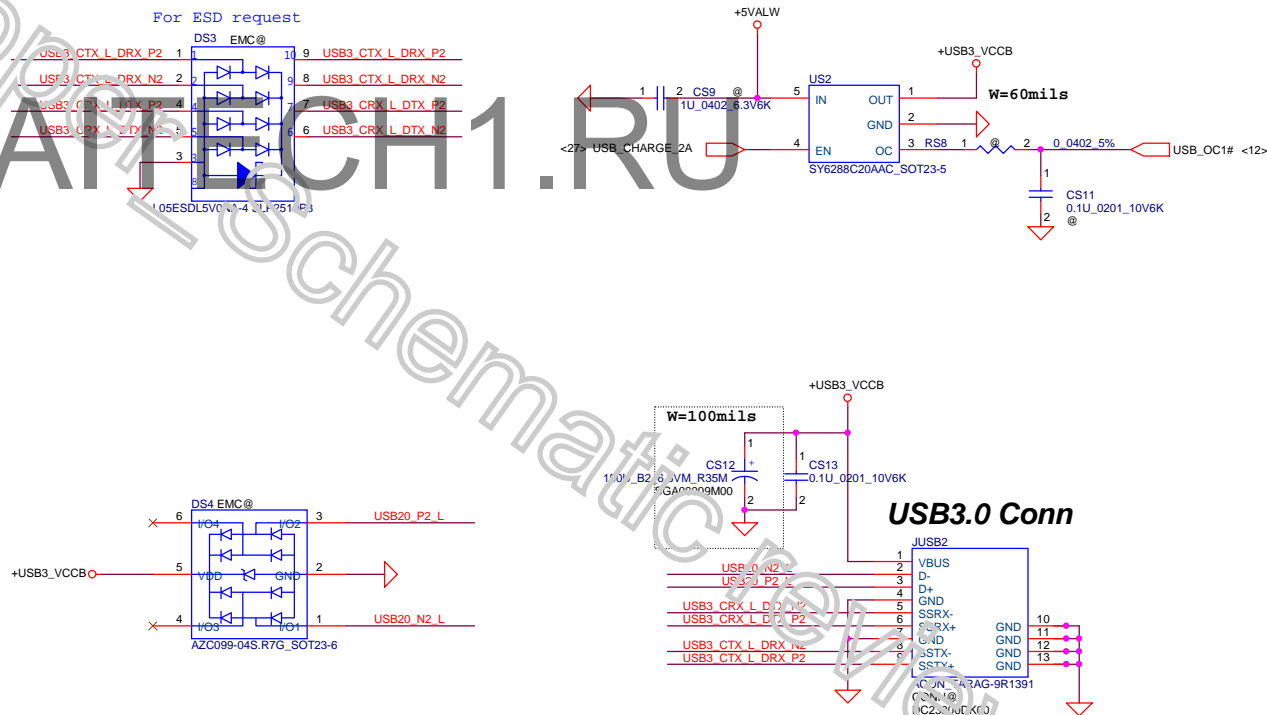
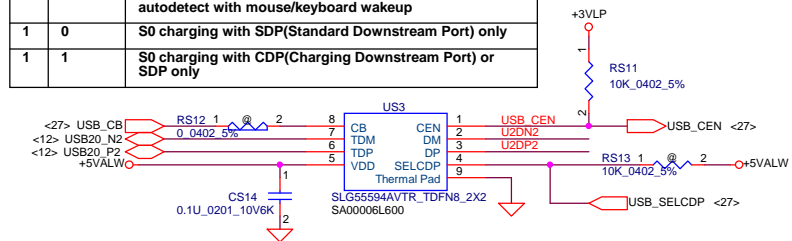


Note: (A4WAS PVT)
Delete 0 ohm path for DFX request
Avoid Common Mode Choke Shift
LS6 EMC@



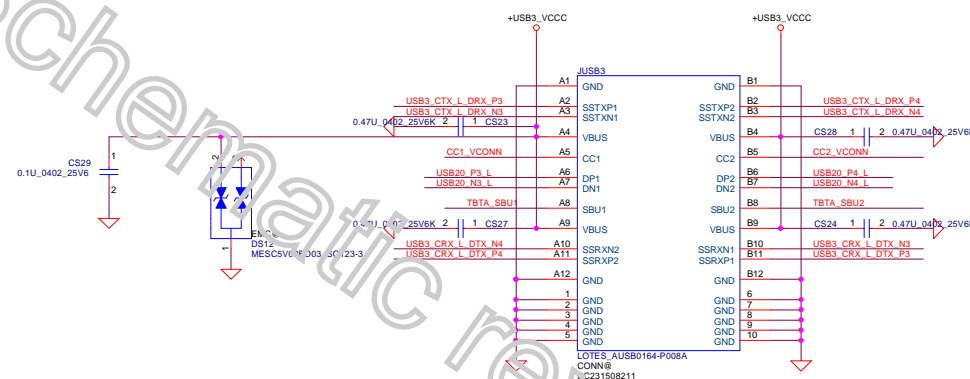
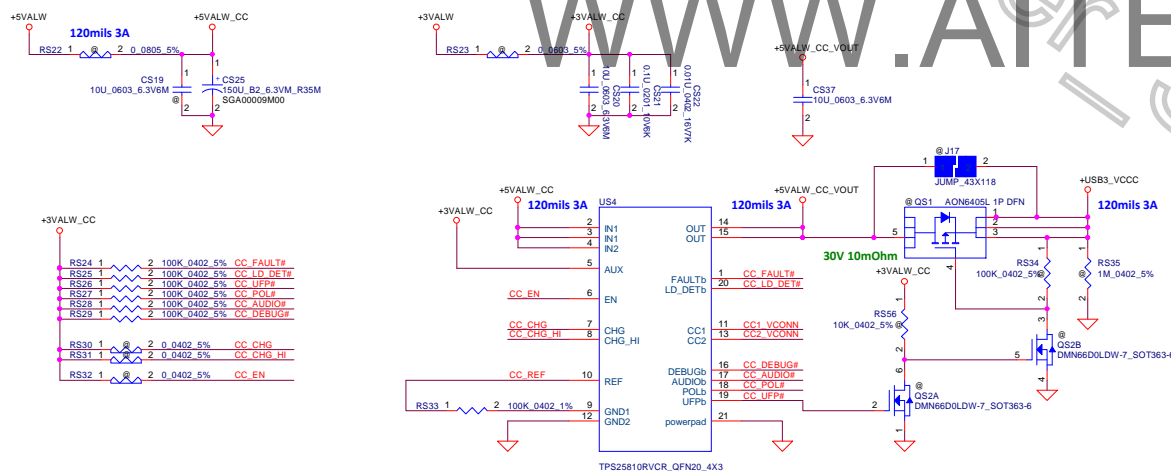
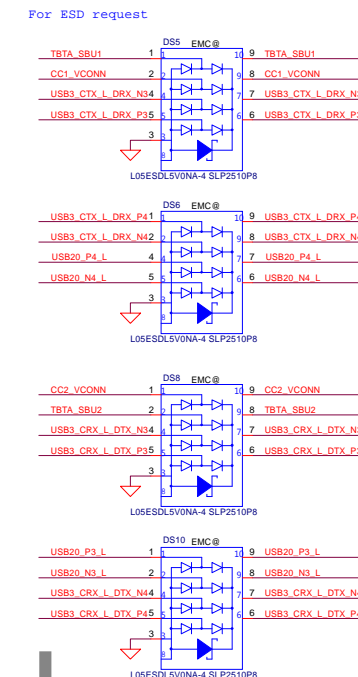
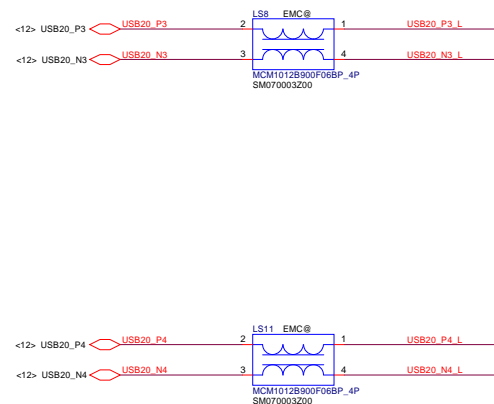
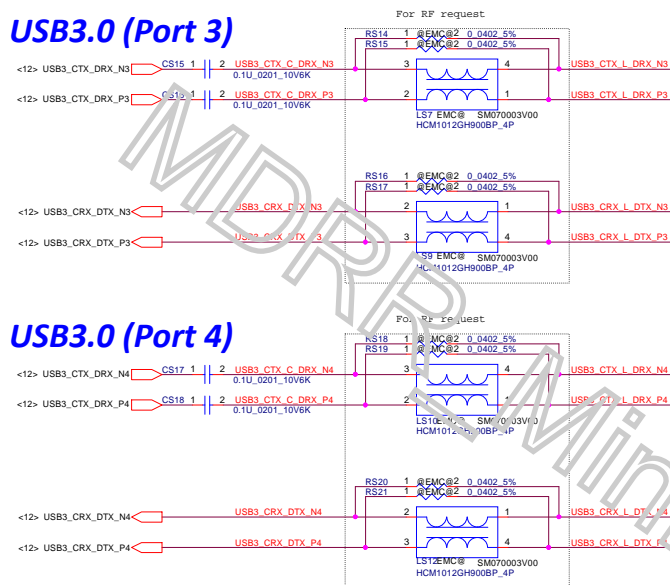
USB Host Charger

CB	SELCDP	
0	X	DCP(Dedicated Charging Port) autotdetect with mouse/keyboard wakeup
1	0	S0 charging with SDP(Standard Downstream Port) only
1	1	S0 charging with CDP(Charging Downstream Port) or SDP only



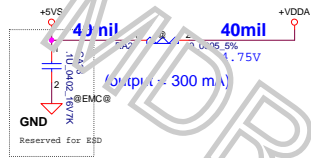
Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date	2015/10/21	Deciphered Date	2016/06/21	Title	USB3.0 Conn/USB B		
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				B3ZMS LA-D591P		2.0	
				Date: Wednesday, February 24, 2016		Sheet 24 of 45	

USB3.0 (Port 4)



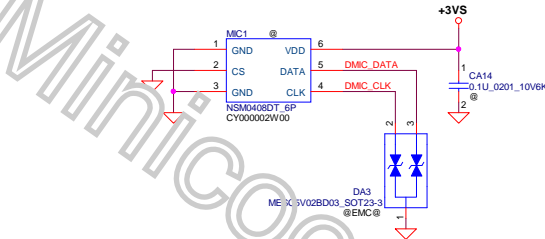
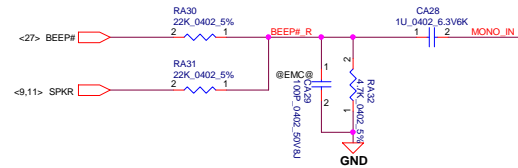
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Issued Date	2015/10/21	Deciphered Date	2016/06/21	Doc. No.	1013/3/5 POWER	Rev. 2.0
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				Date:	Wednesday, February 24, 2016	Sheet 25 of 45

Audio

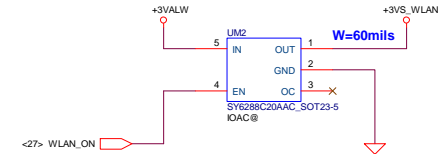
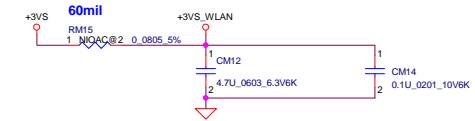


Digital MIC Singal-MIC
MIC BOM upload by Audio Team

DMIC_CLK_1 RA11 1 2 0.0402 5% DMIC_CLK
DMIC_DATA_1 RA12 1 2 0.0402 5% DMIC_DATA

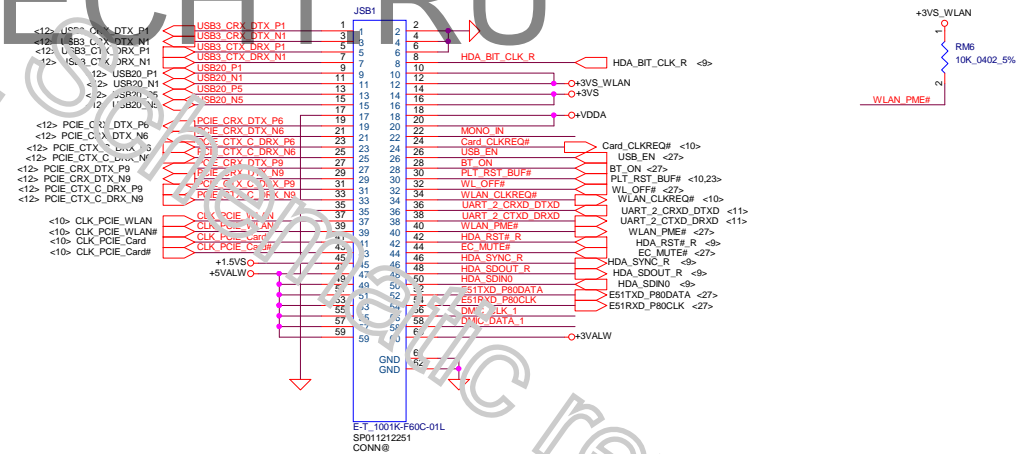


Wireless LAN

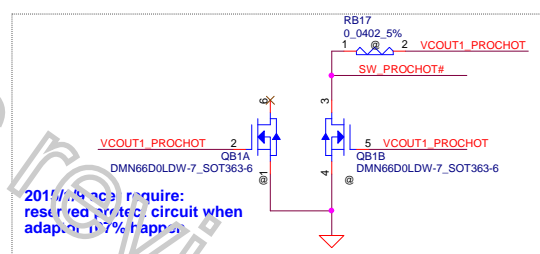
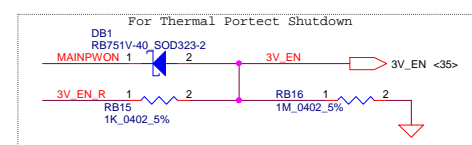
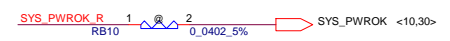
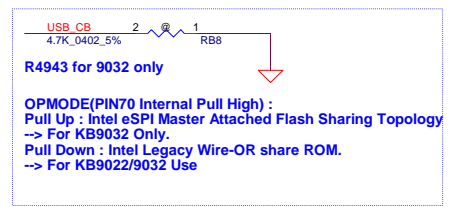
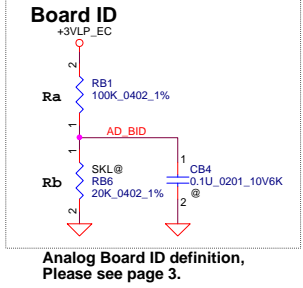
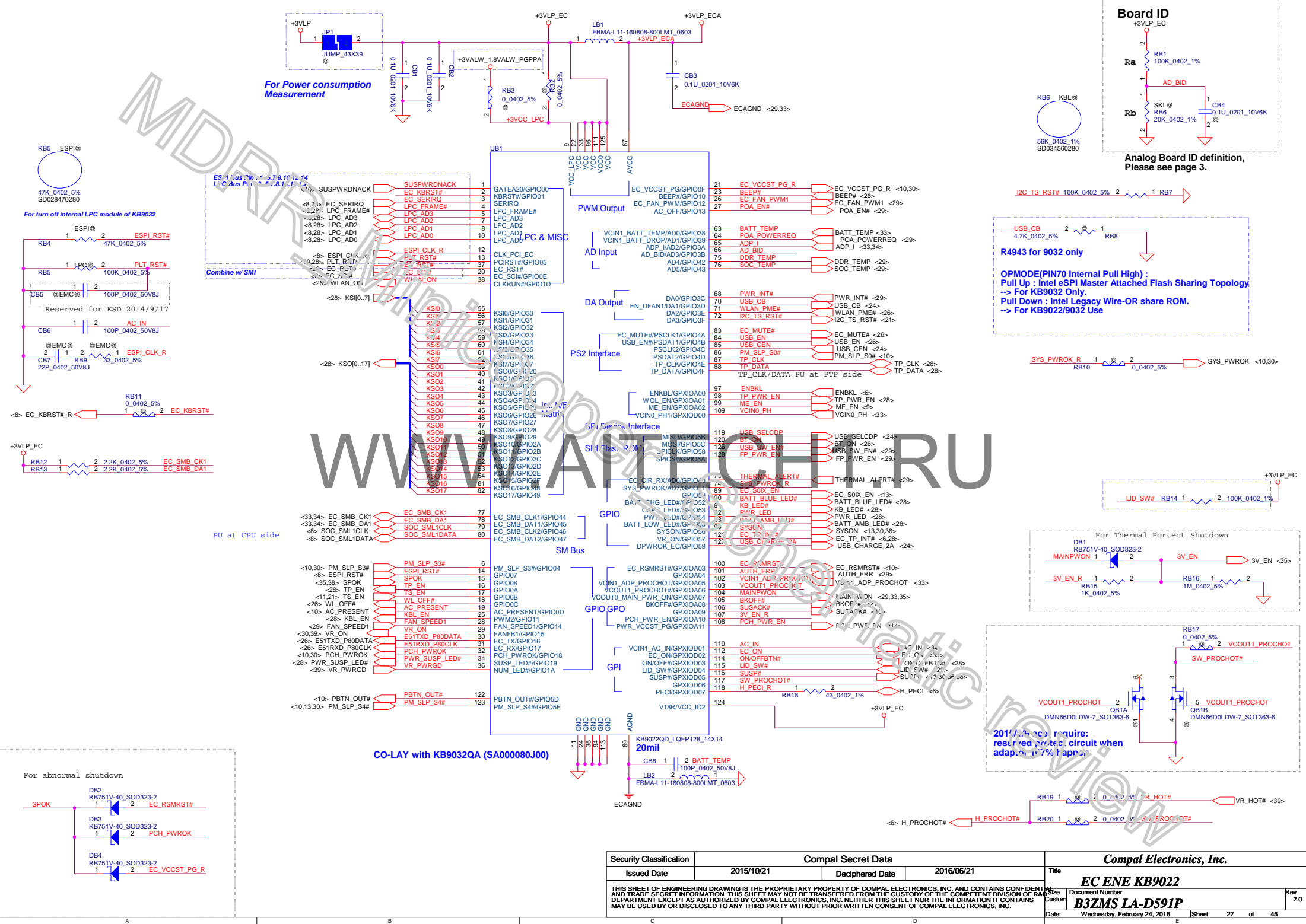


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60pin BTB Conn.

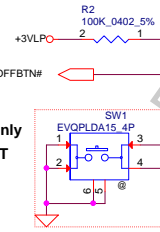


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				P29-CasaRead/RTS5229
				Document Number
				Rev 2.0
				Date: Wednesday, February 24, 2016
				Sheet 26 of 45



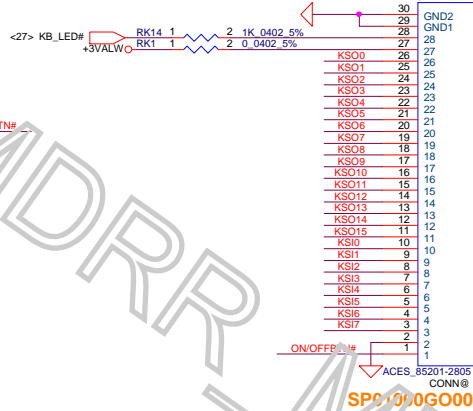
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Issued Date		2015/10/21		Deciphered Date		2016/06/21		Title		EC ENE KB9022	
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Wednesday, February 24, 2016		Sheet		27		of		45			

ON/OFF BTN



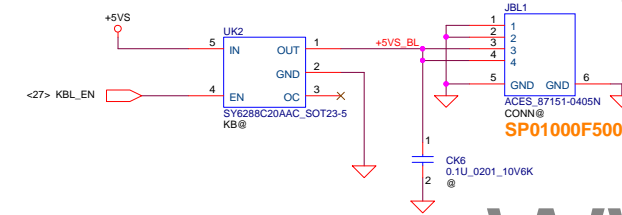
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KSIO[0..17] <27>

KB Conn.



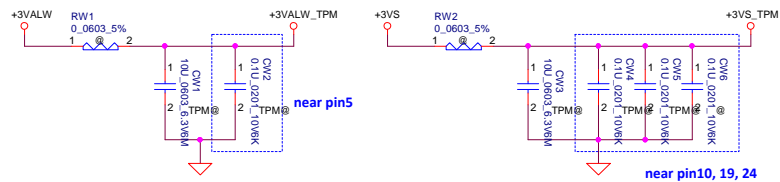
SP01000G000

KB BackLight Conn. Reserve



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TPM Board for 2015



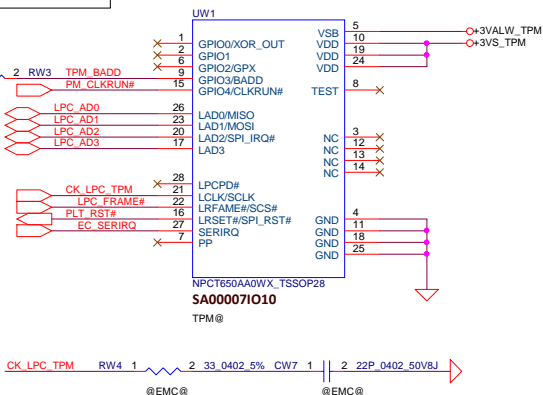
BADD	SELECTION
0	EEh - EFh
* 1	7Eh - 7Fh

GPI03/BADD with Internal PH (default)

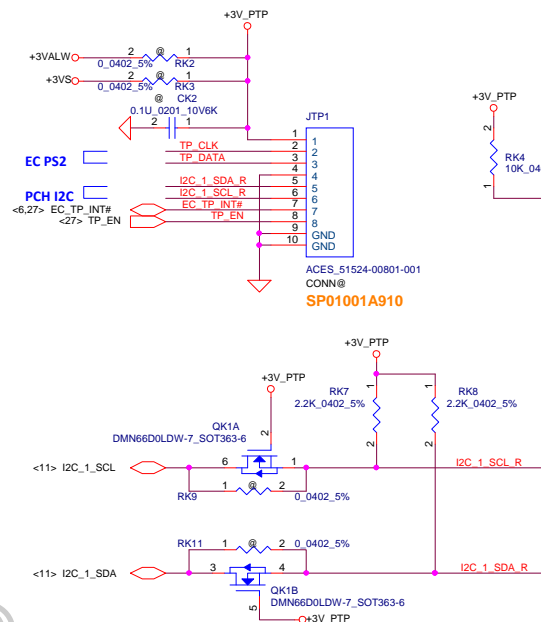
CLCRUN PH 10K to +3VS at PCH side

LPCPD# had internal PH

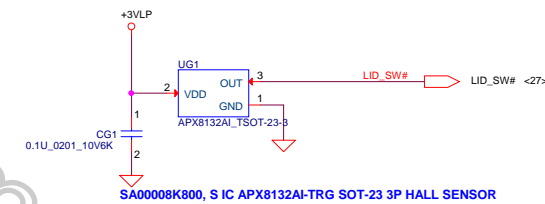
SEIRIQ PH 10K to +3VS at PCH side



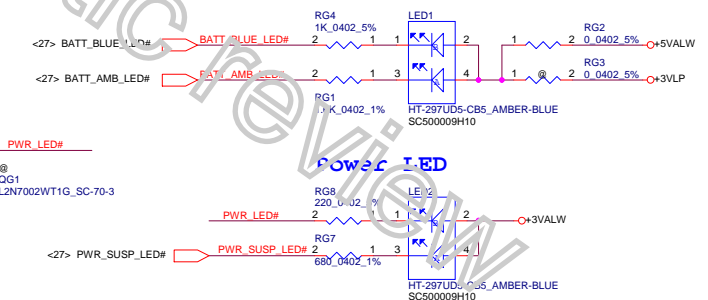
TP/B Conn.



Lid Switch (Hall Effect Switch)



Battery LED



LED

100 1% :SD034100080
150 1% :SD034150080
301 1% :SD034301080
680 1% :SD034680080
120 5% :SD028120080
560 5% :SD028560080
200 5% :SD028200080

UD5: 1.7 ~ 2.3V
(3.3-1.7)/300=5.71 mA
(3.3-2.3)/300=3.57 mA
R min: 100 ohm
R max 700 ohm

CB5: 2.65~3.05V
(3.3-2.65)/50=13.00 mA
(3.3-3.05)/100=5.0 mA
R min: 50 ohm
R max:475 ohm

avoid flash issue when abnormal shutdown

Dual Amber+Blue

LTST-S115TBKF-CA (SC50000C500)

Vf @ 5 mA :

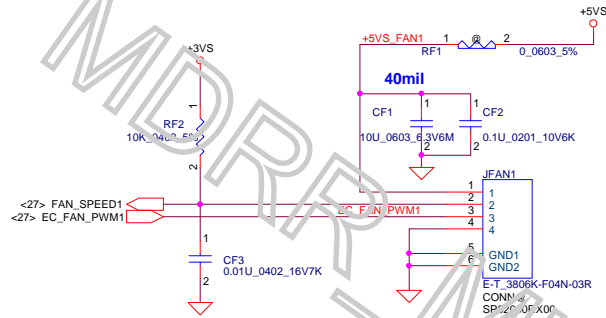
UD5: 1.7 ~ 2.3V
(3.3-1.7)/300=5.71 mA
(3.3-2.3)/300=3.57 mA
R min: 100 ohm
R max 700 ohm

CB5: 2.65~3.05V
(3.3-2.65)/50=13.00 mA
(3.3-3.05)/100=5.0 mA
R min: 50 ohm
R max:475 ohm

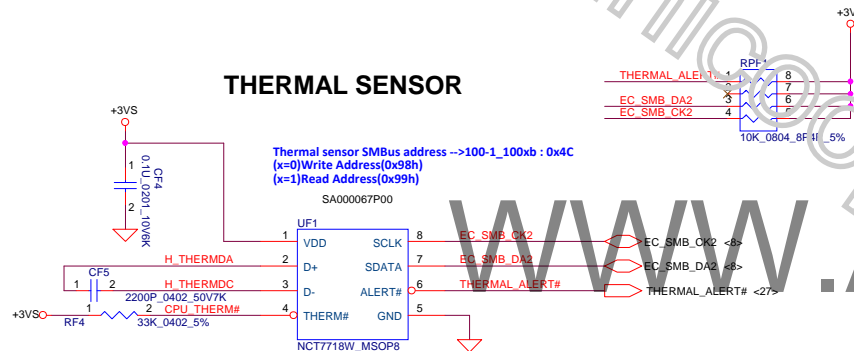
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/10/21	Deciphered Date	2016/06/21	Title	KB & TP & TPM Connector & LED
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				Customer	B3ZMS LA-D591P
				Date	Wednesday, February 24, 2016
				Sheet	28 of 45
				Rev	2.0

FAN

FAN Conn1

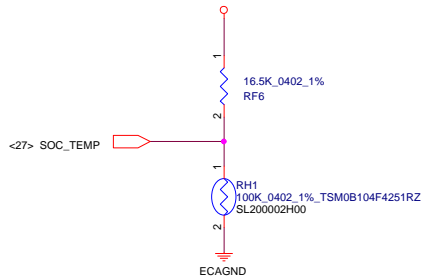


THERMAL SENSOR



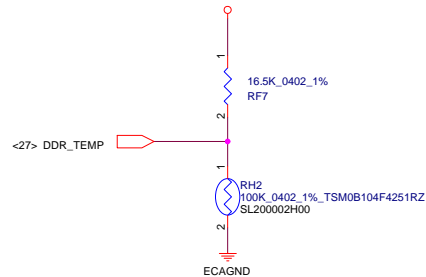
Close to SOC

+3VLP_ECA



Close to DDR

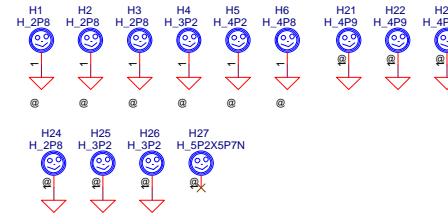
+3VLP_ECA



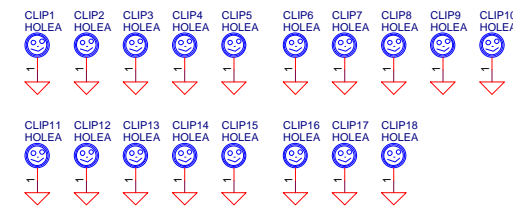
Finger Print GPIO table

Signal Name	Active H/L	Direction	Description
POA_EN#	Low	Host to FPR	to activate the POA functionality
POA_POWERREQ	High	FPR to Host	To request additional power while acquiring/matching fingerprint
PWR_INT#	Low	FPR to Host	trigger power on event to EC
Auth_ERR	High	FPR to Host	to notify EC to error pattern LED or message
USB_SW_EN	High	FPR to Host	Enable USB LS SW
FP_PWREN	High		control FP switch power enable

Screw Hole

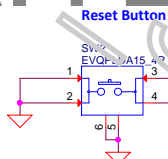


CLIP



Reset Circuit

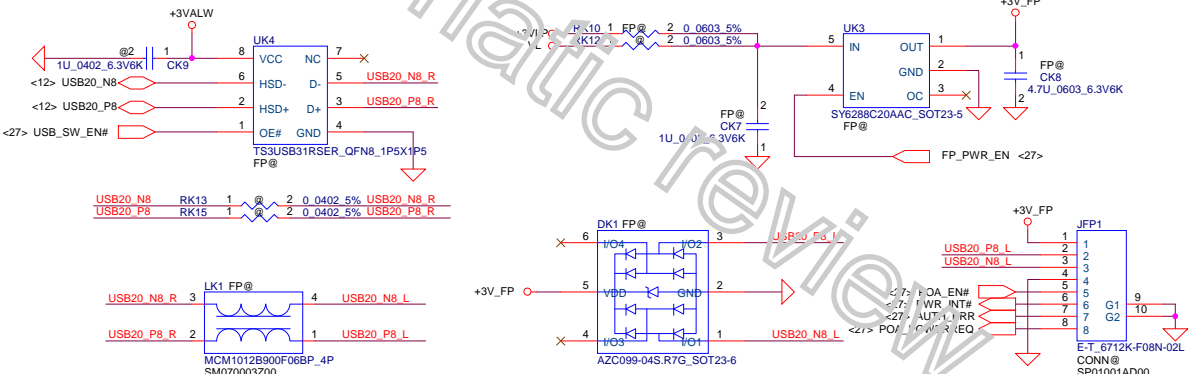
Reset Button



BI_GATE PH to +RTCVCC at PWR side

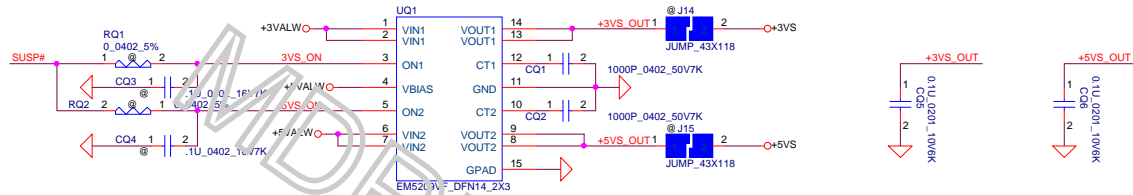


Finger Print

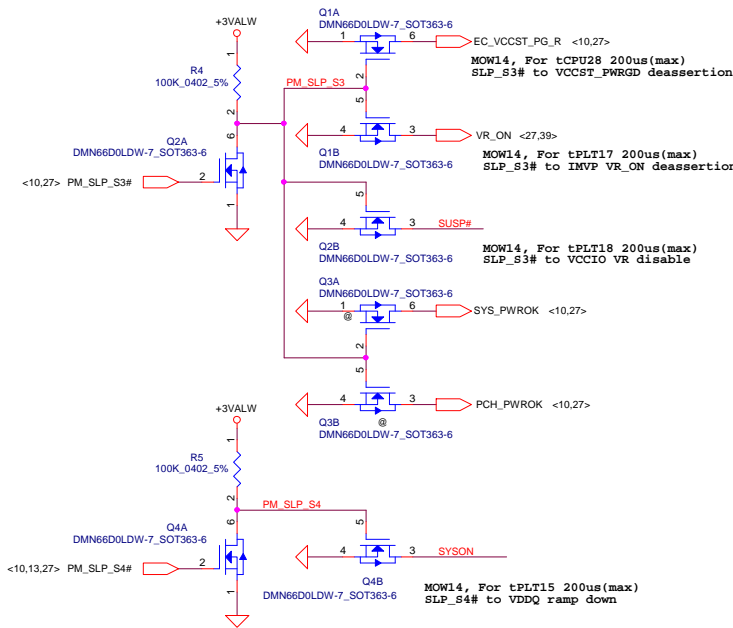


Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date	2015/10/21	Deciphered Date	2016/06/21	Title	FAN & Screw Hole & G-Sensor			Document Number	B3ZMS LA-D591P		
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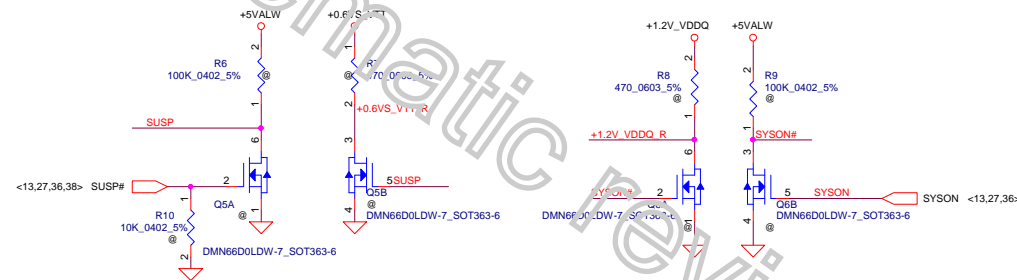
DC Interface

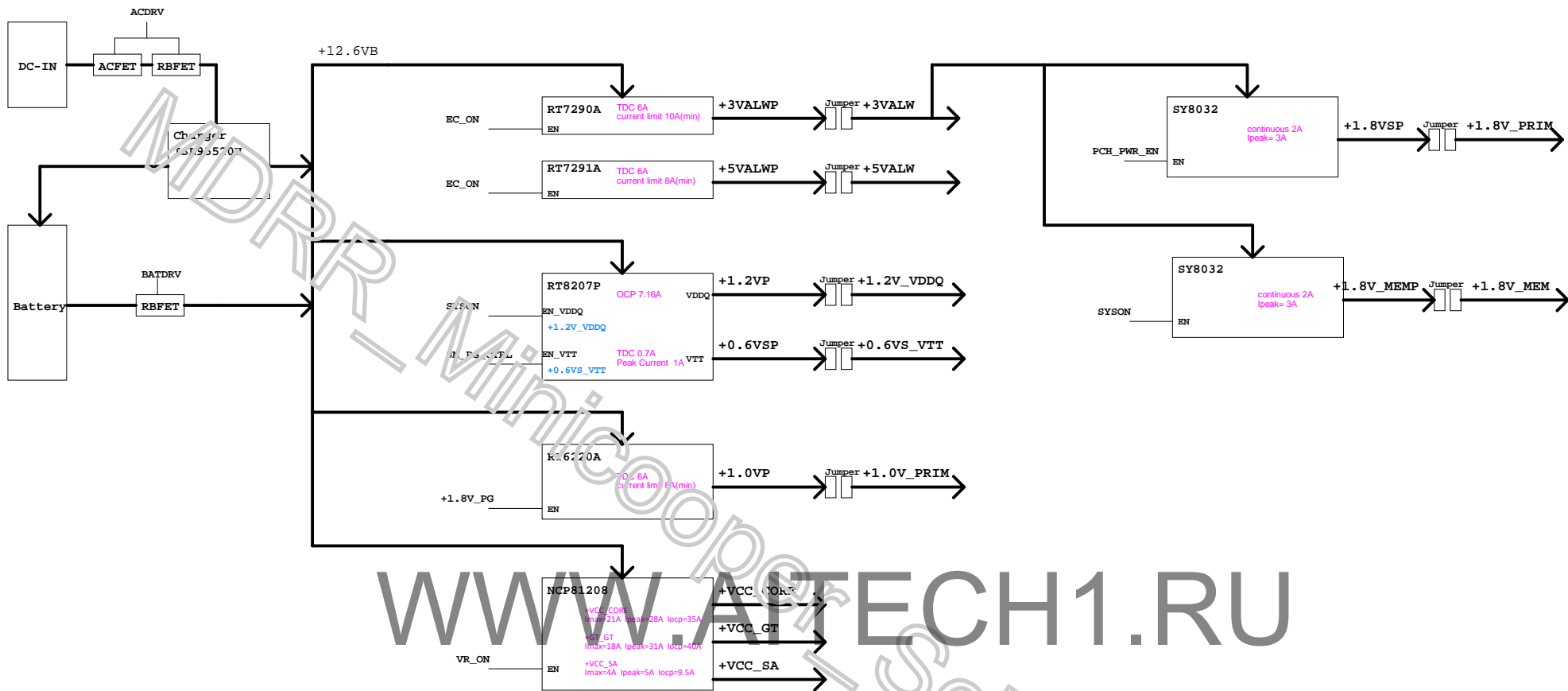


For Power ON/Off Sequence

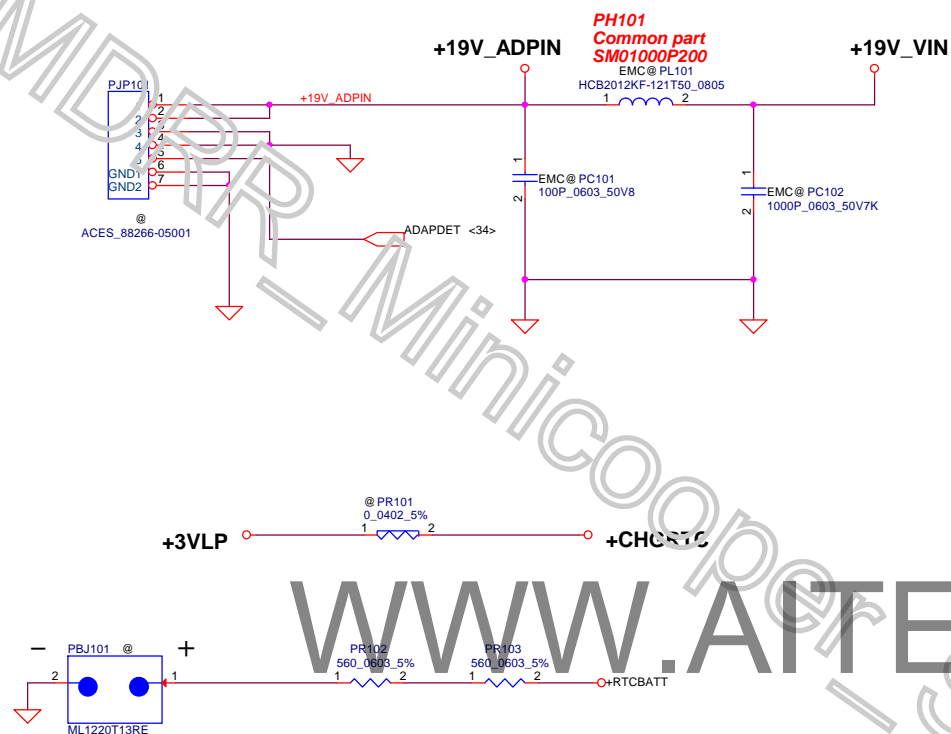


WWW.AITECH1.RU



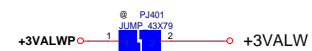
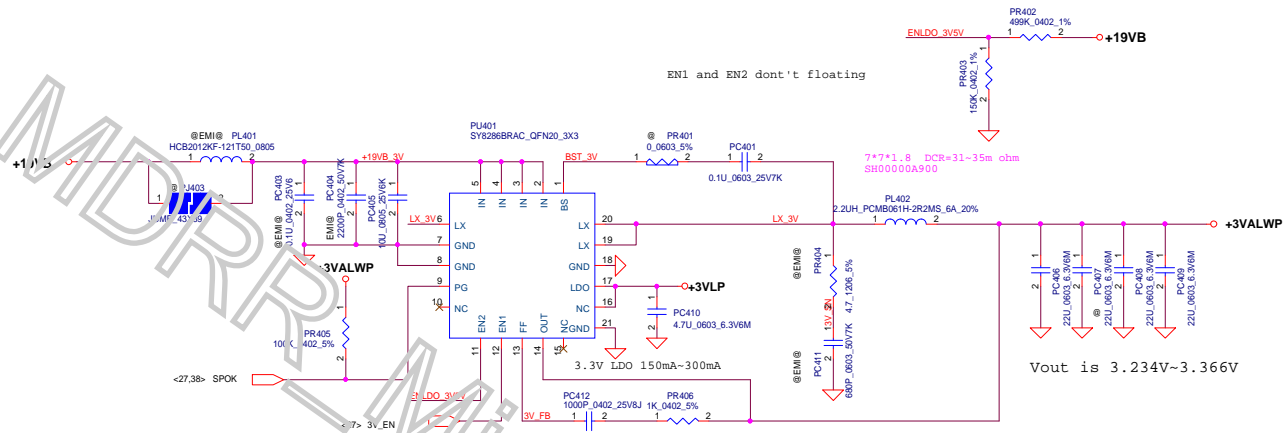


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Size	Document Number			Rev	
	B3ZMS LA-D591P			2.0	
Date:	Wednesday, February 24, 2016	Sheet	31	of	45

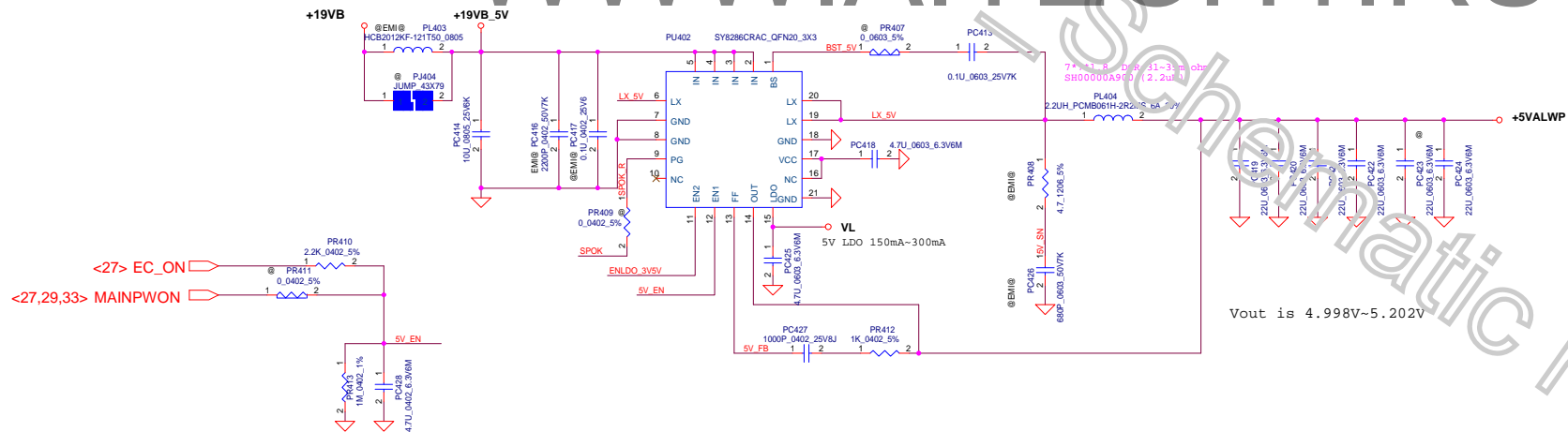


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Date: Wednesday, February 24, 2016				Sheet 32 of 43	





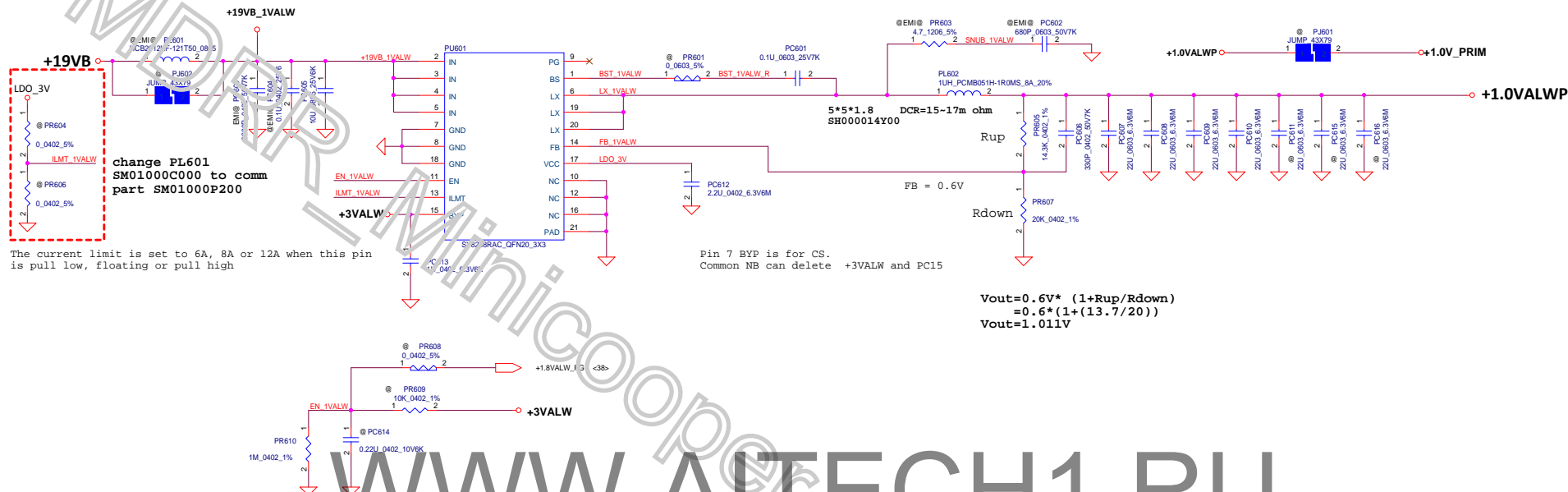
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					LA-C482P
				Date	Sheet 35 of 43

Module model information
SYX196D_V3.mdd

EN pin don't floating
If have pull down resistor at HW side, pls delete PR702



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Size	Document Number	LA-C482P	Rev	2.0
Date:	Wednesday, February 24, 2016	Sheet	37 of	43

VCORE
Imax=21A Ipeak=29A Iocp=35A
LL=2.4mV/A

GT
Imax=18A Ipeak=31A Iocp=40A
LL=3.1mV/A

VCCSA
Imax=4A Ipeak=4.5A Iocp=9.5A
LL=10.3mV/A

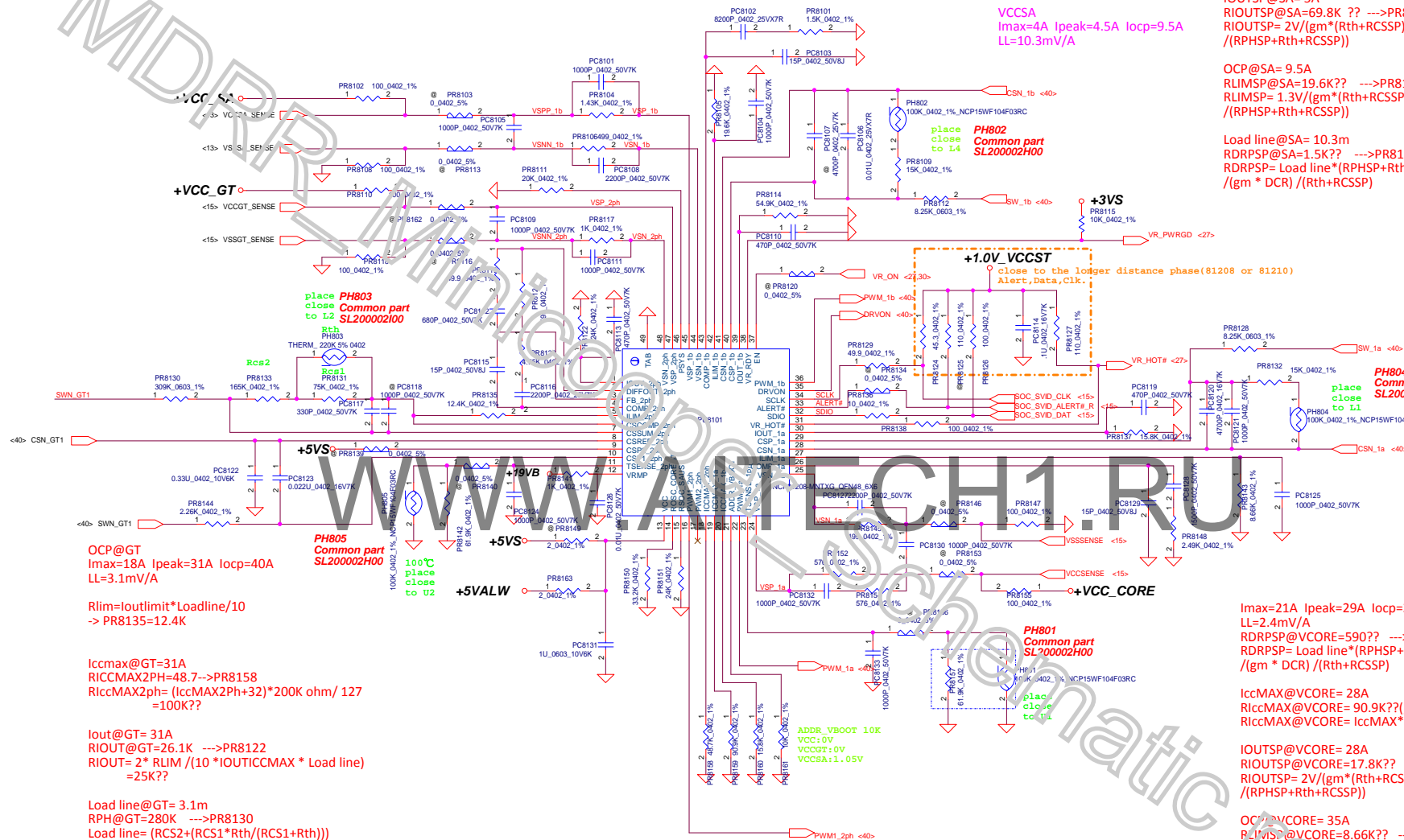
Imax=4A Ipeak=4.5A Iocp=9.5A
LL=10.3mV/A
IccMAX@SA= 5A

RiccMAX@SA= 15.8K ---->PR8160
RiccMAX@SA= IccMAX*2V/10uA/64A

IOUTSP@SA= 5A
RIOUTSP@SA=69.8K ?? ---->PR8114
RIOUTSP= 2V/(gm*(Rth+RCSSP))*IccMAX*DCR
/(RPHSP+Rth+RCSSP))

OCP@SA= 9.5A
RLIMSP@SA=19.6K?? ---->PR8105
RLIMSP= 1.3V/(gm*(Rth+RCSSP))*IoutLIMIT*DCR
/(RPHSP+Rth+RCSSP))

Load line@SA= 10.3m
RDRPSP@SA=1.5K?? ---->PR8104
RDRPSP= Load line*(RPHSP+Rth+RCSSP)
/(gm * DCR) /(Rth+RCSSP)



OCP@GT
Imax=18A Ipeak=31A Iocp=40A
LL=3.1mV/A

Rlim=Ioutlimit*Loadline/10
-> PR8135=12.4K

Iccmax@GT=31A
RiccMAX2PH=48.7-->PR8158
RiccMAX2ph= (IccMAX2Ph+32)*200K ohm/ 127
=100K??

Iout@GT= 31A
RIOUT@GT=26.1K ---->PR8122
RIOUT= 2* RLIM /(10 *IOUTICCMAX * Load line)
=25K??

Load line@GT= 3.1m
RPH@GT=280K ---->PR8130
Load line= (RCS2+(RCS1*Rth/(RCS1+Rth)))
*IOUTTOTAL * DCR/RPH=92.95??

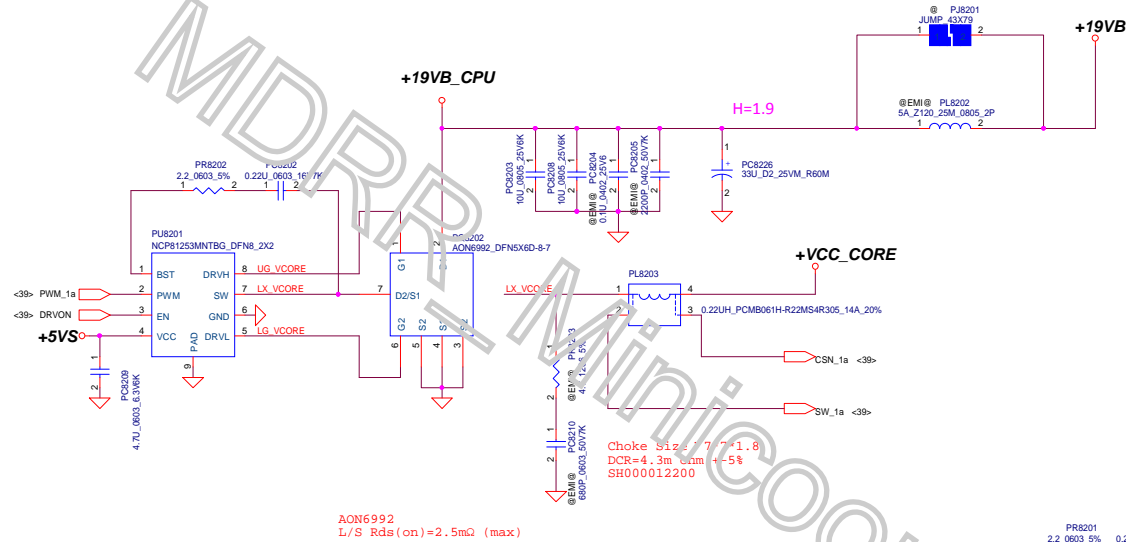
Imax=21A Ipeak=29A Iocp=35A
LL=2.4mV/A
RDRPSP@VCORE=590?? ---->PR8152
RDRPSP= Load line*(RPHSP+Rth+RCSSP)
/(gm * DCR) /(Rth+RCSSP)

IccMAX@VCORE= 28A
RiccMAX@VCORE= 90.9K??(應該是87.6K) ---->PR8159
RiccMAX@VCORE= IccMAX*2V/10uA/64A

IOUTSP@VCORE= 28A
RIOUTSP@VCORE=17.8K?? ---->PR8137
RIOUTSP= 2V/(gm*(Rth+RCSSP))*IccMAX*DCR
/(RPHSP+Rth+RCSSP))

OCP@VCORE= 35A
RLIMSP@VCORE=8.66K?? ---->PR8143
RLIMSP= 1.3V/(gm*(Rth+RCSSP))*IoutLIMIT*DCR
/(RPHSP+Rth+RCSSP))

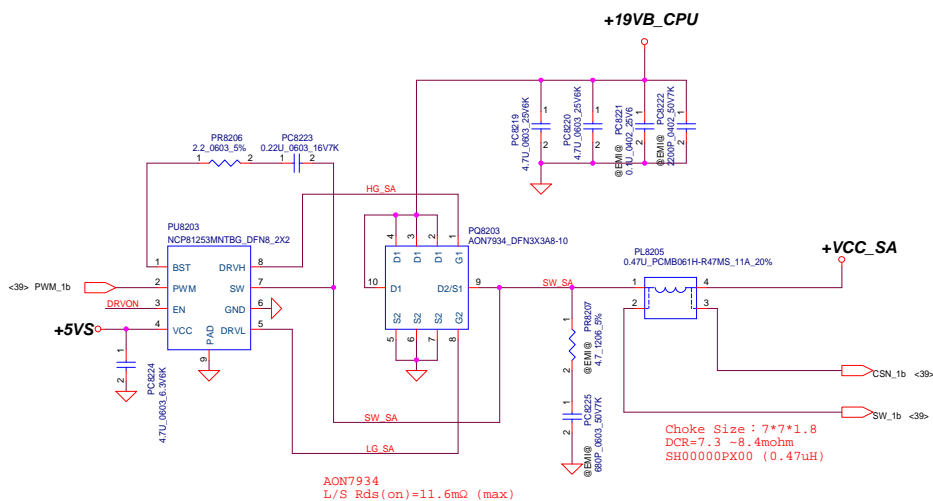
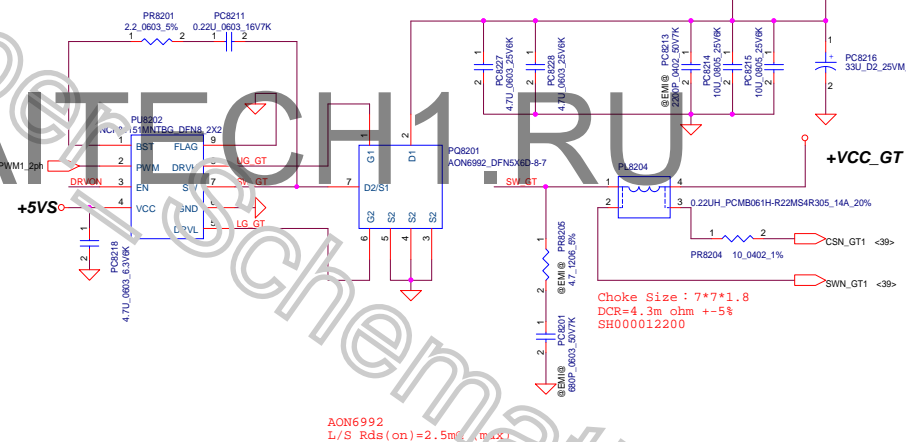
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Size	Document Number	LA-C482P	Rev	2.0
Date:	Wednesday, February 24, 2016	Sheet	39 of	43



VCORE
Imax=21A Ipeak=29A Iocp=35A
LL=2.4mV/A

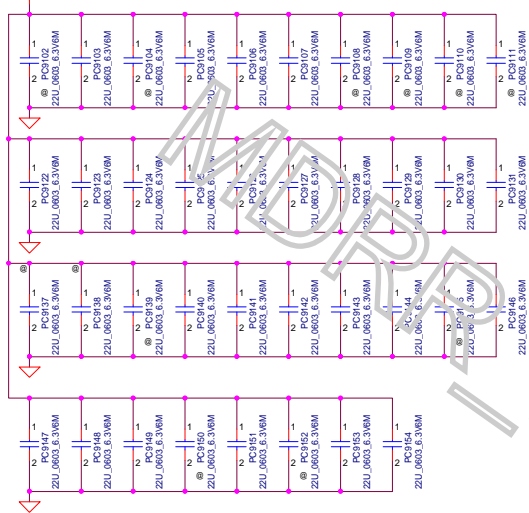
GT
Imax=18A Ipeak=31A Iocp=40A
LL=3.1mV/A

VCCSA
Imax=4A Ipeak=4.5A Iocp=9.5A
LL=10.3mV/A

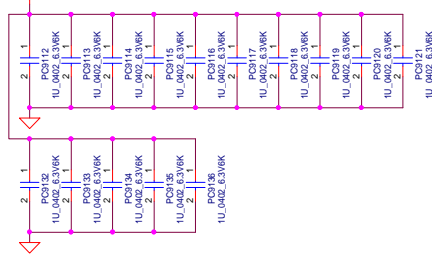


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				Document Number
				LA-C482P
				Rev
				2.0
				Date: Wednesday, February 24, 2016
				Sheet 40 of 43

+VCC_CORE



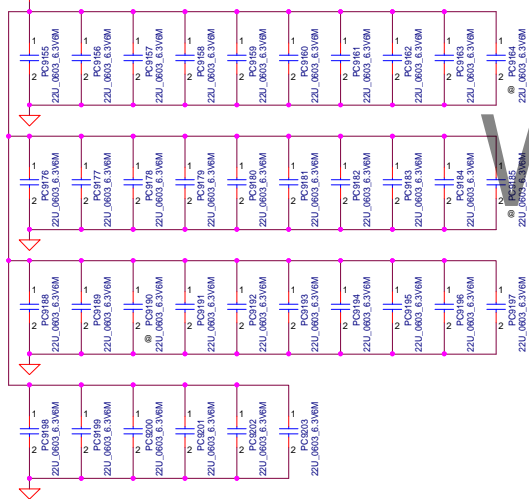
+VCC_CORE



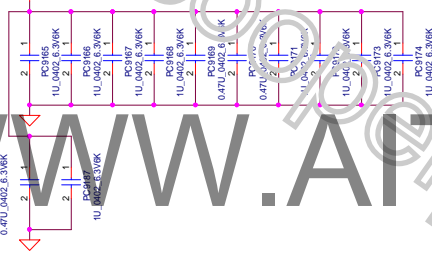
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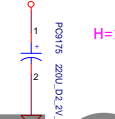
+VCC_GT



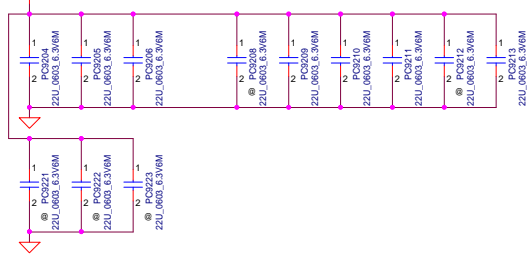
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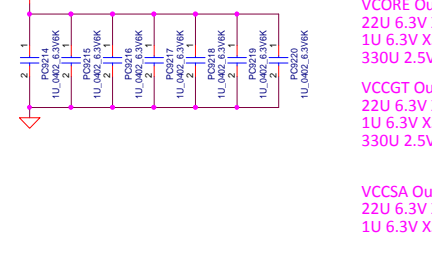
+VCC_GT



+VCC_SA



+VCC_SA



330U_D3_2.5VY_R6M-->H=1.4
SGA00006A00

330U_D2_2V_Y-->H=1.9
SGA00009500

2015/09/15

VCCORE Output Cap :
22U 6.3V X5R 0603 * 38
1U 6.3V X5R 0402 * 15
330U 2.5V D2 ESR6M * 1

VCCGT Output Cap :
22U 6.3V X5R 0603 * 36
1U 6.3V X5R 0402 * 12
330U 2.5V D2 ESR6M * 1

VCCSA Output Cap :
22U 6.3V X5R 0603 * 13
1U 6.3V X5R 0402 * 7

2015/10/21

VCCORE Output Cap :
Backside 22U 6.3V X5R 0603 * 13
Primary 22U 6.3V X5R 0603 * 16
22U 6.3V X5R 0402 * 15

VCCGT Output Cap :
Backside 22U 6.3V X5R 0603 * 13
Primary 22U 6.3V X5R 0603 * 20
220U 2V D2 * 1
0.47U 6.3V X5R 0402 * 3

VCCSA Output Cap :
Backside 22U 6.3V X5R 0603 * 4
Primary 22U 6.3V X5R 0603 * 3
1U 6.3V X5R 0402 * 7

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Size	Document Number	LA-C482P			Rev
		2.0			
Date:	Wednesday, February 24, 2016	Sheet	41	of	43

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P36	change	11/19	Jims_Liu	avoid material shortage	PL502 change SH000015N00 to SH00000AA00	
2	P36	change	11/19	Jims_Liu	avoid material shortage	PU501 change SA000096O00 to SA00007IH00	
3	P37	change	11/19	Jims_Liu	for power efficient	PL602 change SH00000TV00 to SH000014Y00	
4	P41	POP	11/19	Jims_Liu	for CPU trancient	22uF (PC9107、PC9131、PC9140、PC9198、PC9199、PC9200) change unpop to SMT	
5	P41	non-POP	11/19	Jims_Liu	for CPU trancient	22uF (PC9190、PC9164、PC9185、PC9111,PC9145, PC9104,PC9108,PC9122,PC9123) change SMT to unpop	
6	P41	change	11/19	Jims_Liu	for CPU trancient	PC9101 change from SGA00009S00_330uF to SGA20221D40_220uF and SMT	
7	P39	non-POP	11/19	Jims_Liu	for CPU trancient	PR8130 change from SD014280380_280Kohm to SD014309380_309Kohm	
8	P39	change	11/19	Jims_Liu	for CPU trancient	PR8122 change form SD034261280_26.1Kohm to SD034240280_24Kohm	
9	P39	change	11/19	Jims_Liu	for CPU trancient	PR8123 change from SD034523180_5.23Kohm to SD034475180_4.75Kohm	
10	P39	change	11/19	Jims_Liu	for CPU trancient	PC8115 change from SE075472K80_4700pF to SE075222K80_2200pF	
11	P39	change	11/19	Jims_Liu	for CPU trancient	PR8114 change from SD034590280_59Kohm to SD00000H880_54.9Kohm	
12	P39	change	11/19	Jims_Liu	for CPU trancient	PC8106 change from SE000000680_8200pF to SE068103K80_0.01uF	
13	P39	change	11/19	Jims_Liu	for CPU trancient	PR8137 change from SD034178280_17.8Kohm to SD034158280_15.8Kohm	
14	P39	change	11/19	Jims_Liu	for CPU trancient	PR8152 change from SD00000080_590ohm to SD034576080_576ohm	
15	P39	change	11/19	Jims_Liu	for CPU trancient	PR8154 change from SD000000J00_665ohm to SD034576080_576ohm	
16	P38	change	11/19	Jims_Liu	change to common part	PL701 change from SH00000XB00 to SH000001S00	
17	P34	change	11/19	Jims_Liu	follow HW 2nd source	PQ301、PQ308 change from SB000000Q80 to SB000000ST00	
18	P39	change	11/24	Jims_Liu	Save production time	PR8139、PR8120 change from 0 ohm to P_short	
19	P37	change	11/24	Jims_Liu	for HW require	PR605 change from SD034137280_13.7K to SD000000Q80_14.3K	
20	P37	change	11/24	Jims_Liu	for audio noise	PC8219、PC8220 change from SE000000QK00_10uF to SE000013880_4.7uF	
21	P38	change	11/25	Jims_Liu	for PU701 pull high	PR701 change from SD028470280_47Kohm to SD028100480_1Mohm	
22	P39	change	11/27	Jims_Liu	co-lay	add PR8163_SD000005V00 co-lay 5Valw PR8194_SD000005V00 change to unpop	
23	P37	change	11/30	Jims_Liu	more place for CPU_GT	PJ601 change from JUMP_43X118 to JUMP_43X79	
24	P35	change	12/08	Jims_Liu	for efficiency	PL402 change from SH00000LT00_2.2uH_H1.5 to SH00000A900_2.2uH_H1.8	
25	P40	change	12/08	Jims_Liu	for efficiency	PL8205 change from SH000018B00_47uH_H1.5 to SH00000PX00_47uH_H1.8	
26	P34	change	01/11	Jims_Liu	for EMI request	remove unpop PL301(SH00000PB00) & PJ301	
27	P34	change	01/13	Jims_Liu	for power debug	add PJ301	

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LA-C482P			Rev. 2.0	
Wednesday, February 24, 2016			15:08 42 of 43	

Version Change List (P. I. R. List)

Page 1/3 for

Item	Page#	Function	Date	Request Owner	Issue Description	Solution Description	Rev.
1	ALL	PWR	9/14		combine power schematic 0914	combine power schematic 0914	
2	P.20	HW	9/14		remove DDR cap	remove CD150,CD151	
3	ALL	HW	9/14		Compare connector list	Compare connector list	
4	P.24,25	HW	9/30		USB cap change to B2	CS12,CS25 change to SGA00009M00	
5	P.29	HW	9/30		remove for assembly change	Remove SW3,SW4	
6	P.23,26	HW	10/1		JUMP change to R-short for placement	J1,J17 change to RM2,RA2	
7	P.23	HW	10/1		SATA cap change size for placement	CM7,CM8,CM9,CM10 change from 0402 to 0201	
8	ALL	HW	10/1		swap pin for layout routing	Swap LY1,LY2,LY3 LY4 ,LS5,LS4,LS12,RPC5	
9	P.26	HW	10/2		USB3 re-driver update P/N for new version	US5 change from SA00005OR00 to SA00005OR30	
10	P.28	HW	10/5		For KB/B debug	Add RK15,RK16	
11	P.26	HW	10/5		update FPC pin define	update JSB1 pin define	
12	P.9,11	HW	10/5		change Project_ID&RAM_ID pin	pin_U1-4 for RAM_ID , pin_P1-4 for Project_ID	
13	P.9,11	HW	10/5		Change USB30 ESD part for ESD request	Add DS5,DS6,DS8,DS10	
14	P.8	HW	10/7		PC schematic checklist	RPC1 change from 1k to 2.2k	
15	P.12	HW	10/7		for layout request	Swap RPC9,RPC10	
16	ALL	HW	10/7		For DE/EMI request	Change LX2,LS4-LS12 from 0805 to 0504	
17	P.23	HW	10/7		For layout co-layer	Add RM16,RM17	
18	P.10	HW	10/7		Remove ME reset pad	Remove CC119,CLRP3	
19	P.10	HW	10/7		Add 60k pull up for XTAL_BIASREF	Reserve RC158	
20	P.10	HW	10/7		update Crystal P/N	update YC1,YC2	
21	P.11	HW	10/7		Combine net to RPC8	Combine DGPU_PWR_EN to RPC8	
22	P.13	HW	10/7		Add Cap for load switch output	Add CC51	
23	P.14	HW	10/7		Non-DS3 sequence	Pop RC135 ; unpop RC137	
24	P.21	HW	10/7		Reduce 0ohm part count	Remove RX2,RX7	
25	P.23	HW	10/7		Change SSD power cap value	CM5 change from 4.7uF to 10uF	
26	P.8	HW	10/7		Combine parts	QC1 change to SB00000DH00	
27	P.25,28	HW	10/7		Combine parts	QG1,QS2 change to SB00000S700 (SOT323)	
28	P.28	HW	10/7		modify KB schematic	RK14 change to 1K , remove RK12,RK13	
29	P.29	HW	10/7		modify FAN schematic	Remove RF3	
30	P.30	HW	10/7		Add Cap for load switch output	Add CC53,CC55	
31	ALL	PWR	10/8		Combine power schematic 1008	Combine power schematic 1008	
32	P.25,28	HW	10/8		Combine parts	QG1,QS2 change to SB00000ST00	
33	P.29	HW	10/12		update screw hole	H24,H25,H26 change to PTH	
34	P.25	HW	10/13		combine USB into ESD diode	delete DS7,DS9 , USB into DS5,DS6,DS8,DS10	
35	P.25	HW	10/13		Change Type-C cap volt (6.3V&16V -> 25V)	Change CS26,CS29 to 25V	
36	P.27	HW	10/14		Add BT_ON on EC pin120	Add BT_ON on EC pin120	
37	ALL	HW	10/15		For EMI request	Remove CG10,CG2,CS8,LY1,LY2,LY3,LY4	
38	P.26	HW	10/15		update JSB1 pin define	USB_OC0# change to BT_ON	
39	ALL	PWR	10/15		Combine power schematic 1015	Combine power schematic 1015	
40	P.25	HW	10/15		update Type-C schematic	Remove CS26 , update JUSB2 pin define	
41	ALL	PWR	10/15		Combine power schematic 1015B	Combine power schematic 1015B	
42	P.27	HW	10/16		update EC pin define for KB backlight	pin27 <-> pin72	
43	P.26	HW	10/16		update JSB1 pin define	delete one GND pin , add +3.3V WLAN	
44	ALL	HW	10/19		remove test point	CFG10-15,T30,T6	
45	P.14	HW	10/19		add cap to +3VALW_DSW	Add CC86	
46	P.28	HW	10/19		remove 0ohm	remove RK10	
47	ALL	HW	10/19		Change 0-ohm to R-short for part count	RM11,RC122,RC124,RS12,RQ1,RQ2,RC49,RC81,RC83,RC111,RC115,RC113,RC114,RC125,RC127,RC128,RC131,RC132,RC134,RC136,RC144,RC145,RC118,RC119,RC123,RC126,RC133	
48	ALL	PWR	10/19		Combine power schematic 1019	Combine power schematic 1019	
49	ALL	PWR	10/20		Combine power schematic 1020	Combine power schematic 1020	
50	P.13	PWR	10/21		BOM update	pop RC112 , unpop UC8,CC49,CC43,CC45	
51	P.14	PWR	10/21		BOM update	pop RC129 , unpop RC130	

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Issued Date	2015/10/21	Deciphered Date	2016/06/21	Title	HW P.I.R (1/3)
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Date:	Wednesday, February 24, 2016	Sheet	43	of	45

Item	Page#	Function	Date	Request	Owner	Issue Description	Solution Description	Rev.
52	ALL	PWP	10/22			combine power schematic 1021C	combine power schematic 1021C	
53	P.10	HW	10/22			part count	unpop RC85	
54	P.13	HW	10/22			power source cap added	pop CC45,CC49	
55	P.21	HW	10/22			use USB interface touchscreen	unpop RX10,RX11	
56	P.28	HW	10/22			LED interface update	pop RG5 ; unpop RG6,QG1	
57	P.8,9	HW	10/22			update BOM config	RC31 -> LPC@ , RC32 -> TPM@ , RC54 -> EMC@	
58	P.11,18,19	HW	10/22			update BOM config -> X76@	UV1-4,RC150-157	
59	P.3	HW	10/22			update BOM config -> CPU	QJ8Q@,SR2EU@,SR2EY@,QJKK@	
60	P.27	HW	10/22			update Board ID	RB6 change to 0ohm	
61	ALL	HW	10/23			2.2uF change Part Number to SD000008880	CC54,CC60,CD28,CD53,CD51,CD22,CD48,CD37,CD46,CD24,CD44,CD42	
62	P.11,12	HW	10/23			Part count reduce	unpop RC50,RC51,RC92,RC93,CC24,CC25,CC26,CC27,CC28,CC29,CC30,CC31	
63	P.25	HW	10/23			Part count reduce	unpop CS19,CW6,CC109,CC110	
10/21	A gerber	10/21 A gerber	10/21 A gerber	10/21 A gerber	10/21 A gerber	10/21 A gerber	10/21 A gerber	
64	P.7	HW	11/11			UC2 X1 code	UC2 change from SA00005U600 to SA00007UR00	
65	P.26	HW	11/11			US5 change symbol to TI (small thermal pad)	US5 change symbol to TI (small thermal pad)	
66	P.28	HW	11/11			LED pin error	swap LED1,LED2	
67	P.25	HW	11/11			Type-C schematic update for CC_UFP#	QS2 change from singal-N to dual-N	
68	P.25	HW	11/12			Type-C schematic update for VCC	CS29 change from 10uF to 0.1uF	
69	P.26	HW	11/16			move U3 re-driver to S/B	remove US5 from M/B	
70	P.26	HW	11/16			Change BT1 COM1 for cost	JSB1 vendor change to ENTERY	
71	P.26	HW	11/16			WLAN_PME# pull at M/B side	RM6 desgin in M/B side	
72	P.26	HW	11/17			update JSB1 pin define	reduce +5VALW*1 , add +VDDA*1	
73	P.25	HW	11/17			Combine BOM	DS12 change to SCA00002M00 (same as S/B)	
74	P.8,28	HW	11/17			Remove TPM schematic	Remove TPM schematic	
75	P.25	HW	11/17			update Type-C schematic	Replace RS36 by J17 ; unpop QS1,QS2,RS34,RS56	
76	P.11	HW	11/17			remove SCI Pull-up	Remove RPC8 pin1	
77	P.6	HW	11/17			SOC_OCC# connect to GND	SOC_OCC# connect to GND	
78	ALL	HW	11/18			part count reduce	RC129,RB17,RC112,RA11,RA12,RC35,RS30,RS31,RS32,RG3,RG11,RC84,RC104,RC106,RX4,RC140,RS22,RS23,RF1,RC110,RC135,RX12,RX13	
79	P.26	HW	11/18			part count reduce	RA13 remove	
80	P.28	HW	11/18			unpop test power button	unpop SW1	
81	P.27	HW	11/18			Board ID update	RB6 change from 0-ohm to 12KOhm	
82	P.27	HW	11/18			update EC GPIO table	XB1_EN change from pin27 to pin25	
83	P.27	HW	11/18			update EC GPIO table	remove EC_LID_OUT#	
84	P.7	HW	11/19			change net[SM_PG_CTRL] PU power	RC25 PU change from +3VALW to +3VS	
85	P.8	HW	11/19			part count reduce	unpop RC76,RC27,RC30	
86	P.9,26	HW	11/19			remove PCH DMIC signal	remove RA7,RA8,net[PCH_DMIC_CLK],net[PCH_DMIC_DATA]	
87	P.30	HW	11/19			change to correct location by naming rule	CC53,CC55 change to CQ5,CQ6	
88	P.13	HW	11/19			combine parts -> 0.1uF 0201	CC46 change from 0403 to 0201	
89	ALL	HW	11/19			combine parts -> 10uF 0603	CC106,CS19,CS30,CS37	
90	P.26	HW	11/25			Use dual U3 re-driver for U3 issue	US5 group on M/B	
91	P.26	HW	11/26			Add AC cap between 1st 8713 & 2nd 8713	Add CS33,CS34	
92	ALL	PWR	11/26			Combine power schematic	Combine power schematic	
93	P.6	HW	11/26			Intel Debug	RC6,RC7,RC8,RC19 change to RC16 (unpop)	
94	P.26	HW	11/26			update JSB1 pin define for EMI request	pin8 <-> pin60	
95	P.6	HW	11/26			reserve PU +3VS for EC SCI# (for kabylake?)	Reserve RC159	
96	P.26	HW	11/27			Vendor recommend : update REXT PD value	RS53 change from 3.83k-ohm to 4.99k-ohm	
97	ALL	PWR	11/30			Combine power schematic	Combine power schematic 1130	
98	P.10	HW	12/1			Add PD for PLT_RST_BUF#	Add RC53	
99	P.26	HW	12/2			Remove U3 re-driver	Remove US5 group	
100	P.29	HW	12/2			Add PU for Thermal sensor SMBus	Add RPF1 , remove RF5	
101	P.27	HW	12/2			Add BOM config for ENE request (PLT_RST# PD)	RB5 100K for LPC@ , 47K for ESPI@	
102	P.28	HW	12/2			remove debug KB pin	remove RK15,RK16	

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Issued Date	2015/10/21	Deciphered Date	2016/06/21	Title	HW P.I.R (2/3)
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				Rev	2.0
				Date	Wednesday, February 24, 2016
				Sheet	44 of 45

Item	Page#	Function	Date	Request	Owner	Issue Description	HW	Solution Description	Rev.
103	P.13	HW	12/3			change load switch CT value		CC39 change from 10pF to 470pF	
104	ALL	PWR	12/8			Combine power schematic 1208		Combine power schematic 1208	
105	P.26	FW	12/31			Add PME PU on M/B		Add RM6	
106	P.14	FW	12/31			Cost reduce		unpop UC10,CC112	
107	P.29	HW	1/5			Add POA schematic		Add POA schematic	
108	P.28	HW	1/11			Change Battery LED power source to +5VALW		unpop RG3 ; pop RG2	
109	ALL	PWR	1/13			Combine power schematic 0111		Combine power schematic 0111	
110	P.13	HW	1/13			Factory issue		unpop CC52	
111	P.28	HW	1/18			LED R-value change		RG7->680ohm ; RG8->220ohm	
112	P.3	HW	1/19			Add Kabylake CPU P/N		Add SA00009QM10,SA00009PJ30	
113	P.27	HW	1/19			update project ID		RB6 change from 12K-ohm to 15K-ohm	
114	P.29	HW	2/15			update screw hole		H4 change from 2P8 to 3P2	
115	P.27	HW	2/15			update project ID		RB6 change from 15K-ohm to 20K-ohm	
116	P.29	HW	2/17			reserve 0-ohm for FP USB signal		reserve RK13,RK15	
117	P.28	HW	2/18			Combine Part Number		RG8 change from SD034220080 to SD028220080	
118	P.28	HW	2/19			LED value change		RG1 1.1k -> 1.6k ; RG4 1.6k -> 1k	
119	P.28	HW	2/19			HDML/FDCR test result		RY11 change from 4.99k-ohm to 4.75k-ohm	
120	P.29	HW	2/19			update BOM config		RK10 change to FP@	
121	P.27	HW	2/19			update BOM config		Add RB6=56K for Kabylake	

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				Date	Wednesday, February 24, 2016	2.0
				Sheet	45	of 45